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Subcontractor Report

Low-Cost Glass and Glass-Ceramic Substrates for Thin-Film Silicon Solar Cells

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January 25, 2001

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Cornell University
Ithaca, New York

National Renewable Energy Laboratory

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ABSTRACT

An important factor enabling the economical fabrication of the thin film silicon solar cells is the development of an inexpensive transparent substrate that can be processed at temperatures of 700 to 900 ºC. The rate at which silicon is deposited from chemical vapors increases exponentially with temperature, to achieve a high throughput using low cost precursors, a high substrate temperature is needed. A high substrate temperature also minimizes defects in the deposited silicon, as many defects anneal out during deposition. However, available glass substrates cannot withstand temperatures above about 600 ^{o}C, a temperature at which the deposition process is slow and uneconomical. Glass-ceramics, on the other hand can tolerate the high temperatures required for high speed deposition but are generally neither transparent nor matched to the thermal expansion of silicon. Under the contract, novel glass ceramic substrates were fabricated by Corning's experimental glass making laboratory that were transparent (permitting use as a superstrate) and matched to the thermal expansion of silicon. Cornell carried out the necessary tests to qualify the substrates for solar cell production. It is important to note that Corning Inc. carried out its part of the project without receiving funds under the contract.

Under the contract, Cornell developed several low cost and simple barrier layers and tested their effectiveness both analytically (by SIMS) and by evaluating the electrical characteristics of devices fabricated on barrier coated substrates. Devices fabricated included both majority carrier devices (thin film transistors) and minority carrier devices (p-i-n junction diodes simulating solar cells) using various deposition techniques including the chemical vapor deposition of polysilicon from silane at low pressures (at Cornell U.) and from dichlorosilane at atmospheric pressure (cooperation with Neudeck at Perdue U.). The structure of the films deposited was investigated using TEM and X-ray analysis. Impurity outmigration from the coated and non-coated substrates into these films was studied with novel DLTS methods in which single crystal wafers clamped to the substrate played the role of the deposited thin film. The performance of the minority and majority carrier devices fabricated on barrier coated glass ceramic substrates was found to be identical to that of identical devices fabricated on control substrates of oxidized silicon and fused silica.

EXECUTIVE SUMMARY

The economical production of thin film polycrystalline silicon solar cells requires transparent substrates that can be processed at high (T>700ºC) temperatures because: i) a transparent substrate allows use of the substrate as the cover-glass, eliminating the need for a separate cover and ii) most fabrication processes, including the rapid deposition of polysilicon by the most economical deposition process: chemical vapor deposition (CVD), operate effectively only at high temperatures. No suitable substrates meeting these requirements existed prior to the program. The most heat resistant commercial glass substrate (Corning Code 1737) softens at temperatures above 620 ºC. Fused silica (often referred to as 'quartz') is transparent and meets the temperature requirements but is too expensive to be used in mass production. Moreover, fused silica's thermal expansion coefficient is about 1/5 of that of silicon. Therefore, a polysilicon layer deposited at high temperature will be under a tensile stress at room temperature and crack.

Glass-ceramics are a class of materials that can be formulated to be transparent, resistant to high temperatures and to match the thermal expansion of silicon. The main concern of processing glass-ceramics in conventional semiconductor equipment is that various glass components out-migrating from the substrate might contaminate solar cell material and/or processing equipment.

A barrier layer is therefore required to stop the diffusion of glass components from the substrate into the thin film electronics during high temperature (T≥900 ºC) processing. Using SIMS analysis, the ability of various combinations of silicon nitride and silicon dioxide layers to suppress out-diffusion at 900 ºC was evaluated. Since silicon nitride's properties depend on the deposition process, both low pressure and plasma enhanced chemical vapor deposited (LPCVD and PECVD) SiN_x was investigated. A barrier layer consisting of a single, 1000 Å thick SiN_X and a single, 1000 Å thick SiO_2 layers deposited by either PECVD or LPCVD was found to be sufficient to lower out-migration below the detection limit of SIMS.

To verify these results, a high temperature process was developed to fabricate top gated polysilicon thin film transistors (TFTs) at 900 ºC. These majority carrier devices permit *quantitative* measurement of the mobility of electrons (and holes) in the deposited semiconductor films as well as density of states in the band gap. The latter is the electrically relevant measure of the defects contained in the deposited silicon film. Two variations of the high temperature process were investigated. In the first, polysilicon was deposited directly at 620ºC from silane. In the second, amorphous silicon was deposited at 550 ºC and was then recrystallized at 900 ºC. In all cases, we found that the electrical characteristics of devices fabricated on barrier layer coated glass-ceramic substrates were similar to those measured in devices fabricated in the same run on oxidized silicon and fused silica. A subsequent investigation of the small, but systematic differences between different substrates types showed the surface roughness (higher on barrier coated substrates) rather than difference in the impurity background (e.g. from substrate outdiffusion) accounted for the second order difference in device performance. To investigate the long-term stability of devices fabricated on glass ceramic substrates, we subjected transistors fabricated on these substrates to bias stress tests at elevated temperatures. The electrical characteristics of devices fabricated on glass-ceramics

substrates were found to be very stable indicating that deposited polysilicon films were free from mobile ions. This finding is important as alkali is an important class of impurities that could out-diffuse from the substrate.

A solar cell, being a minority carrier device, shows degraded properties at impurity concentrations too low to be detected by SIMS (Secondary Ion Mass Spectroscopy). To convincingly demonstrate the suitability of glass-ceramic substrates for thin film solar cells therefore required the fabrication of minority carrier test structures on these novel substrates. Solar cells and p-i-n junction diodes were hence fabricated on glass-ceramic substrates and, for comparison, in the same run on fused silica and oxidized silicon substrates as well. Two different approaches were used to fabricate these devices. The dark current voltage characteristics of all cells were measured to evaluate the influence of substrate type (glass-ceramic, fused silica and oxidized silicon) on device performance. The low leakage current and high breakdown voltage observed in solar cells and p-i-n junctions fabricated on glass-ceramic substrates and oxidized silicon show that on both substrates the p-i-n junctions are of high quality. On the other hand, on fused silica substrates the junctions were leaky. The poor junction properties were traced to cracks in the polysilicon, visible both in scanning electron microscope (SEM) and light microscope. Calculations showed that the cracks were caused by the mismatch in the thermal expansion coefficient of silicon and fused silica. After cooling, the silicon film is under tension and prone to cracking. Therefore, apart from its high price, fused silica is not a suitable substrate to deposit and process large area polysilicon devices such as solar cells at high temperatures.

At Cornell, only low pressure CVD (Chemical Vapor Deposition) from silane is available. A two-step process yields very high quality polysilicon (deposition of amorphous silicon at 550^{o}C followed by recrystallization at 900^{o}C), which – because of its low intrinsic defects – is very sensitive to defects introduced by the substrate. On the other hand, the process is slow, limiting the thickness of polysilicon that can be deposited in a typical run to about a micron. To efficiently absorb light, a solar cell needs to be at least several microns thick. Two alternate approaches were therefore used in addition to deposit thicker films. Polysilicon was directly deposited by LPCVD from silane at 620 C, or APCVD from diclorosilane at 900 ºC using a thin LPCVD seed layer. This method was found to yield high quality p-i-n diodes with thick (up to 2 micron) intrinsic layers.

The structure of the deposited films was investigated using a number of analytical techniques: TEM, X-ray diffraction, DOS measurements. This investigation showed that fabricated polysilicon films had average grain size of 100 nm with a predominant (110) orientation. This texture is the preferred for the fabrication of thin film solar cells since it results in grain boundaries with lower electrical activity. The density of mid-gap states in the as-deposited films is ~10^{19} $cm^{-3}eV^{-1}$. Hydrogenation of the films in an ECR plasma reduced the density of midgap states to ~10^{17} $cm^{-3}eV^{-1}$.

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1. Properties of Glass Ceramic Substrates

- Composition

Commercial glass-ceramics (e.g. stove tops) are neither transparent nor thermal expansion matched to silicon. To meet the requirements of transparency and expansion matching, several glass-ceramic compositions were evaluated at Corning Incorporated by Dr. Linda Pinckney. The spinel structure (SiO_2-Al_2O_3-ZnO-MgO-TiO_2, ZrO_2) was selected as having the most promise [1].

The batch materials for the glasses included sand, alumina, zinc oxide, magnesium oxide, titania, zirconia, and barium carbonate. Arsenic oxide and ammonium nitrate were added to fine the glass (remove bubbles) and to minimize color from reduced titania (Ti^{3+}). The batch materials were dry ball milled for one hour and transferred to 1-kg platinum crucibles.

The batches were melted in electric furnaces for 6 hours at temperatures of 1600-1625 º C, cast into patties about 8" x 4" x 0.5", and annealed at 725 º C. Two 3" round samples were core-drilled from each glass patty, and the cores sliced into 2-4 wafers about 1 mm thick. Each wafer was then polished on both surfaces.

The polished wafers were "cerammed" (crystallized) in small electric furnaces. The heat treatment consisted of a 2-hour hold at 800 º C for nucleation followed by a 4-hour hold at 1025 º C to complete crystallization. Because of the ultra-fine microstructure of the glass-ceramic, consisting of 10-15 nm-sized spinel crystals dispersed uniformly throughout a siliceous glass [2], there is essentially no change in surface roughness after ceramming.

Some of the important characteristics of the developed LGA glass-ceramics are presented in Table 1, attached at the end of this report.

- Surface roughness and CMP

A glass-ceramic substrate with a low surface roughness is required to fabricate high quality electronic device such as a thin film solar cell. As fabricated substrates have a roughness of 1.5-1.8 nm- rms. Our preliminary studies showed that Chemical-Mechanical Polishing (CMP) could reduce the roughness of glass-ceramic surfaces to 0.3-0.5 nm rms. A special process was developed at Cornell to polish glass-ceramic and fused silica wafers. However, a detailed investigation of the polished surfaces using both optical microscopy and atomic force microscopy revealed the presence of agglomerated small silica particles, which are one constituent in the proprietary CMP slurry (**Figure 1**). These particles adhered to the surface when the polishing process was stopped and became very difficult to remove after the wafer dried. The presence of these 'bonded' silica particles leads to a non-uniform and unacceptably high surface roughness. Moreover, barrier layers deposited on these surfaces become discontinuous at these particles and do not block the out-diffusion of impurities (see details on the barrier layers in the following section).

Table 1. Characteristics of LGA glass-ceramic.

Coefficient of Thermal Expansion – $37x10^{-7}$ /ºC	
Strain point	- 910 ºC
Density	- 2.76 g/cm^3
Young's modulus	- $13.7x10^6$ psi
Modulus of rupture	- 10.5 ksi
Hardness	- 650 KHN/100
Index of refraction	- 1.566
Plate Durability:	
Weight change in:	
5% HCl, 95 ºC, 24 hrs	-0.021
5% NaOH, 95 ºC, 6 hrs	-0.466
10% HF, 22 ºC, 20 min.	-0.189
10% NH_4FHF, 22 ºC, 20 min.	–0.145
Electrical Properties:	
Dielectric constant, 25 ºC, 1 KHz	- 5.5
DC Vol resistivity, 250 ºC	- 10.4 W·cm.

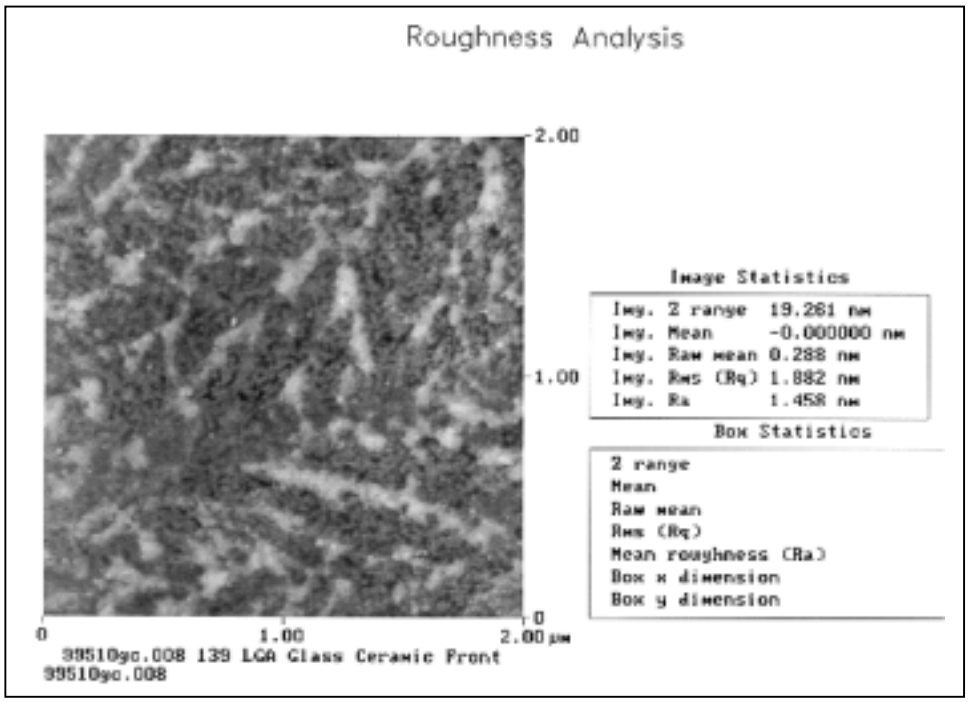


Figure 1. AFM image of the surface of a CMP polished glass-ceramic wafer. Note the presence of silica particles (light spots) that increase the roughness.

To avoid these harmful surface modifications we developed a post-CMP cleaning process. Simple rinsing in DI water does not remove all the particles. We found that the sequence of soft ultrasonic cleaning, DI water cascade rinsing, RCA cleaning [3] and spin drying removes all particles, provided that the wafer is kept in the DI water between all the steps and not allowed to dry until the entire cleaning process is completed.

Booth the CMP polished and cleaned glass-ceramic and the CMP polished fused silica control substrates were carefully inspected, using both optical and atomic force microscopy. The optical microscope reveals areas of silica particle formation, while the atomic force microscope images the surface on a very fine scale and permits to measure the actual surface roughness. No traces of silica particles were found on the polished surfaces of glass-ceramics and fused silica (**Figure 2**) cleaned with the above process.

It should be noted that even after CMP polishing the surface roughness of the glass-ceramics is about 0.7 nm rms versus about 0.3 nm rms for polished fused silica. Since both substrate types were polished identically this difference reflects the different microstructure of the two substrates. The spinel crystals of about 100 Å in size embedded into the silica glass matrix can be clearly seen in the AFM images (**Figures 2 and 3**). Their presence is confirmed by STEM analysis [2]. The difference in hardness between the spinel crystals and the amorphous matrix (essentially SiO_2) results in a different local polishing rate and hence a surface roughness exceeding that of the structurally homogeneous fused silica substrates.

2. Barrier layers

- SIMS and impurity diffusion

Some glass-ceramic components, such as alkali atoms, become very mobile at the elevated temperatures used to process silicon. These mobile ions can migrate from the substrate to the semiconductor film and degrade the device performance [4]. Therefore the glass-ceramic substrates need to be coated with a barrier layer to prevent the out migration of substrate components into the thin film electronics during high temperature processing.

To study the efficiency of various layers as diffusion barriers, we deposited a triple stack of Low Pressure Chemical Vapor Deposition (LPCVD) silicon dioxide and silicon nitride films (100 nm each) onto the polished and cleaned glass-ceramic substrate (**Figure 4**). The advantage of such a design was that even if one SiO_2/SiN_X binary layer failed (due to the presence of pinholes), the other layers would stop out-migration and prevent contamination of the furnace. The coated substrate then was annealed in nitrogen at 900 ºC for 8 hours and Secondary Ion mass Spectroscopy (SIMS) analysis was performed to measure the concentration profiles of glass elements in the layers. As shown in **Figure 5** a single SiO_2 layer fails to stop outdiffusion of most elements. The concentration of all elements, however, drops significantly in the first SiN_x layer and remains at or below the detection level of SIMS in the subsequent layers. This finding indicates that a 100 nm thick SiN_x is sufficient to stop out-diffusion. The top 100 nm thick SiO_2 layer provides a low recombination surface for any subsequently deposited polysilicon films [5].

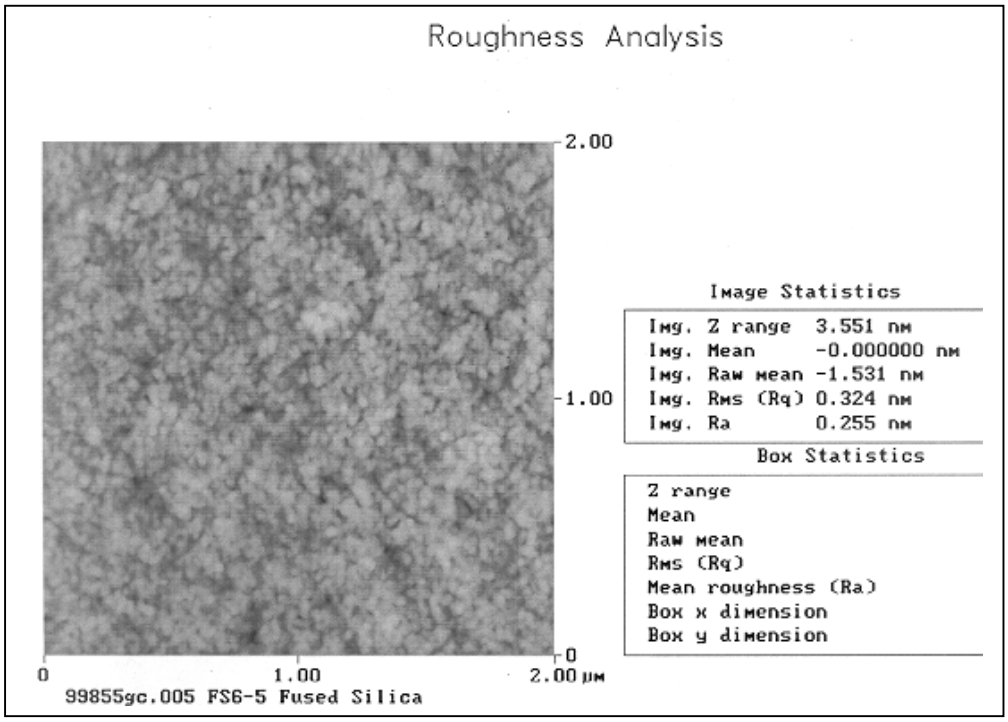


Figure 2. AFM image of the surface of a CMP polished and cleaned glass-ceramic wafer.

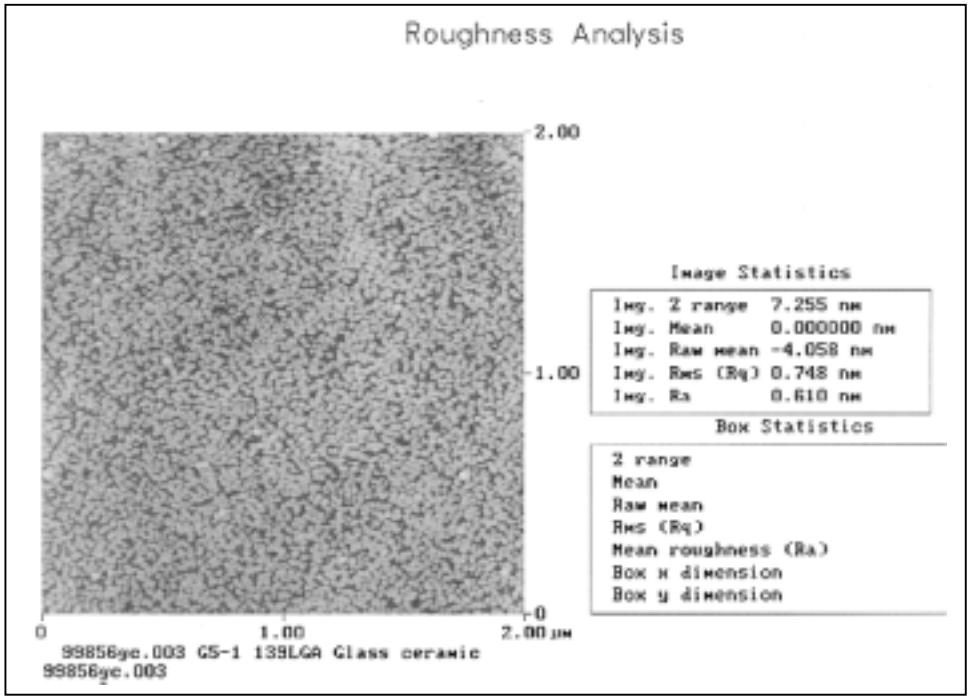


Figure 3. AFM image of the surface of a CMP polished and cleaned fused silica wafer.

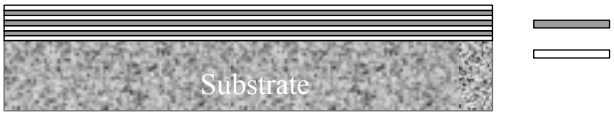


Figure 4. Schematics of the triple SiO_2/SiN_x barrier layer deposited on glass-ceramic substrate.

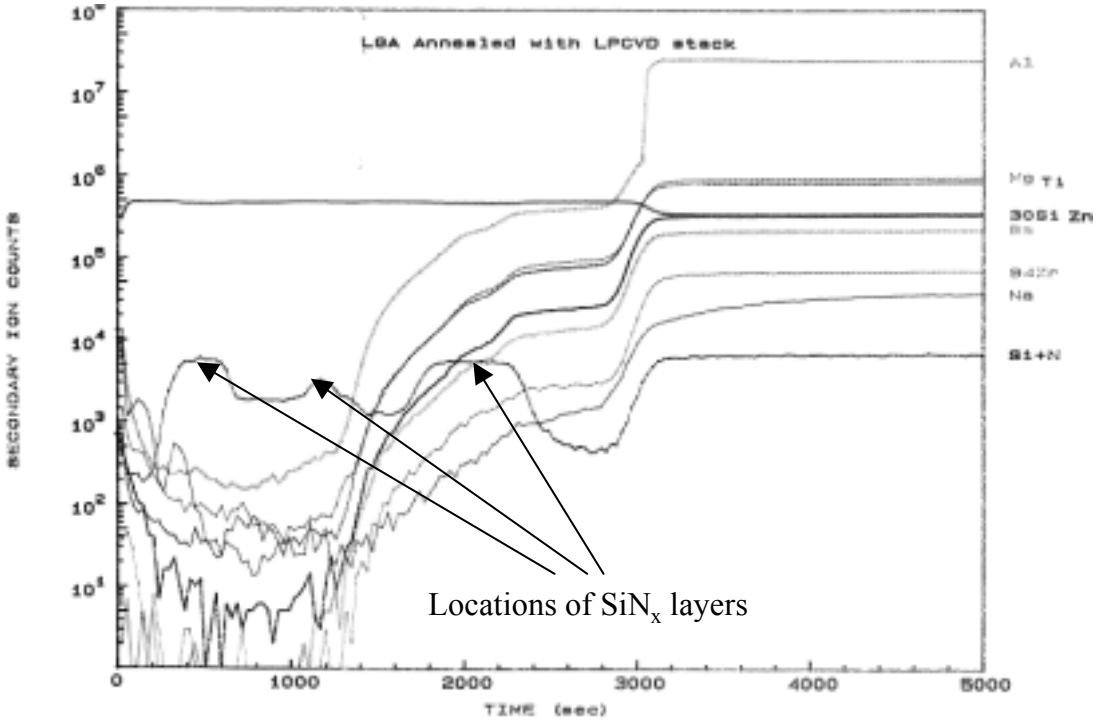


Figure 5. SIMS profile of glass-ceramic components in a triple SiO_2/SiN_x barrier layer. The location of the three SiN_x layers is clearly visible in the Si+N profile.

This triple layer structure, however, was complicated to fabricate. In addition, this barrier had very high surface roughness (over 50 nm rms – the roughness accumulated with the number of layers deposited) and relatively low optical transparency (visibly tinted). Therefore, a new simplified barrier layer for glass-ceramic substrates, consisting of 100 nm of PECVD silicon nitride followed by 100 nm of PECVD silicon dioxide was developed and characterized using SIMS, AFM and optical absorption measurements.

SIMS was used to measure the concentration profiles of glass components in the barrier layer. To induce diffusion, the coated glass-ceramic wafer was first annealed in N_2

at 900 ºC for 4 hours. Elemental profiles were then taken to detect possible out-diffusion of substrate elements (**Figure 6**). As can be seen from the **Figure 6**, the concentration of all elements drops significantly in the nitride layer and remains at the background level in the top silicon dioxide layer. This confirms the above reported finding that a single 100 nm PECVD silicon nitride effectively stops out diffusion from the substrate. Again, a silicon dioxide layer is deposited on top of the nitride to provide the low recombination surface required for any subsequently deposited silicon device layer.

It should be noted that the proper choice of PECVD process parameters for the nitride deposition is critical to avoid darkening the glass-ceramic substrates during barrier layer deposition. Excessive hydrogen can react with titanium, an element contained in the glass-ceramic, and by changing its valence state darken the glass-ceramic [**6**].

- Surface roughness

AFM was used to investigate the surface of the glass-ceramic substrates. Since surface roughness is a very important parameter for any wafer to be used as a substrate for thin film electronics, both bare and barrier layer coated substrates were studied. All available substrates were measured including glass-ceramic, fused silica and oxidized silicon. It was found that deposition of the barrier layer increased the surface roughness of every substrate. Details of our findings are described below.

Figure 7 shows the AFM image of the glass-ceramic surface coated with 'as-deposited' PECVD SiN_x/SiO_2 barrier layer. Notice the increased surface roughness compared to uncoated substrate (1.21 nm rms versus 0.7 nm rms). The AFM image reveals features with average lateral size of 30 nm (**Figure 7**). These features were not found on the surface of bare glass-ceramic wafers (**Figure 2**). To investigate the origin of these features we studied the surfaces of silicon wafers, both bare and coated with barrier layers. While the original surface of the silicon wafer is very smooth (below 0.3 nm rms) (**Figure 8**), the image of a barrier layer coated silicon surface indicates the presence of 'intrinsic' features that increase the roughness to 1.1 nm rms (**Figure 9**). These features are inherent in the structure of the barrier layer and their size (30 nm) does not depend on the surface condition of the substrate, i.e. they are an intrinsic feature of the deposition process. This phenomenon can be explained by considering the nature of the PECVD process. Due to the extreme lack of thermal equilibrium in PECVD, the structure of the deposited film is determined by the process parameters rather than surface conditions. Statistically, the roughness of the barrier layer coated silicon surface is lower than that of glass-ceramics, which suggests both the intrinsic morphology of the barrier layer and the condition of the surface prior to its deposition contribute to the final roughness of a coated substrate.

Another interesting fact is that annealing the deposited PECVD barrier layer increases its surface roughness. After a four hour, 900 ºC anneal in dry nitrogen the mean roughness increased from 1.21 nm rms to 1.66 nm rms. The size of the lateral features on the surface, however, did not change (**Figures 7 and 10**).

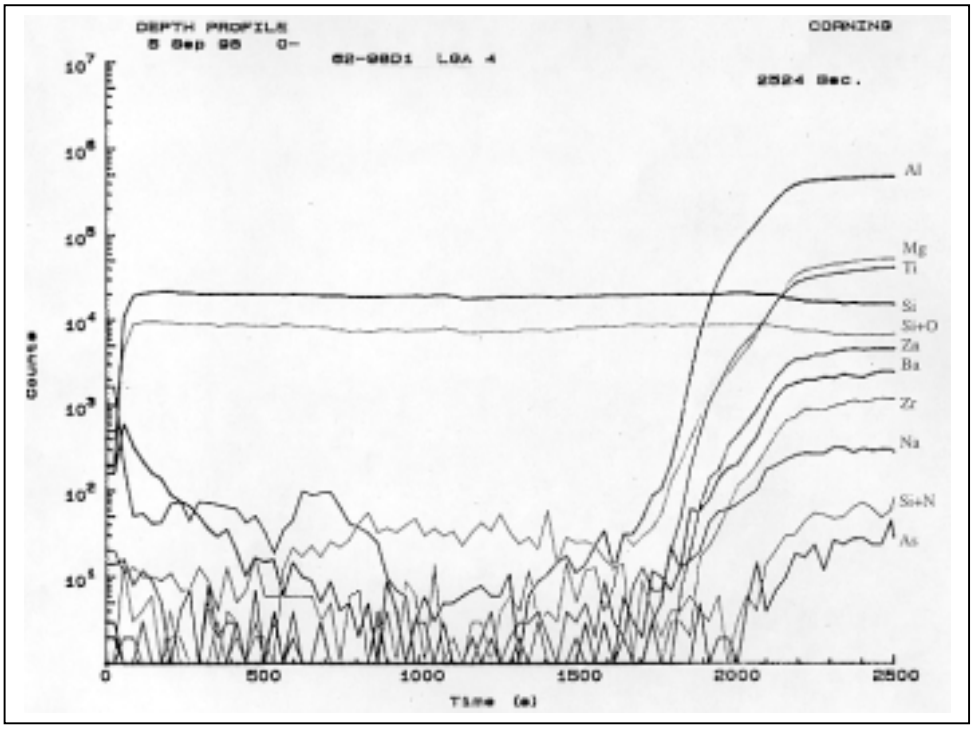


Figure 6. SIMS profile of glass-ceramic components in a PECVD SiN_x/SiO_2 barrier layer. The Si profile is flat as the barrier contains silicon.

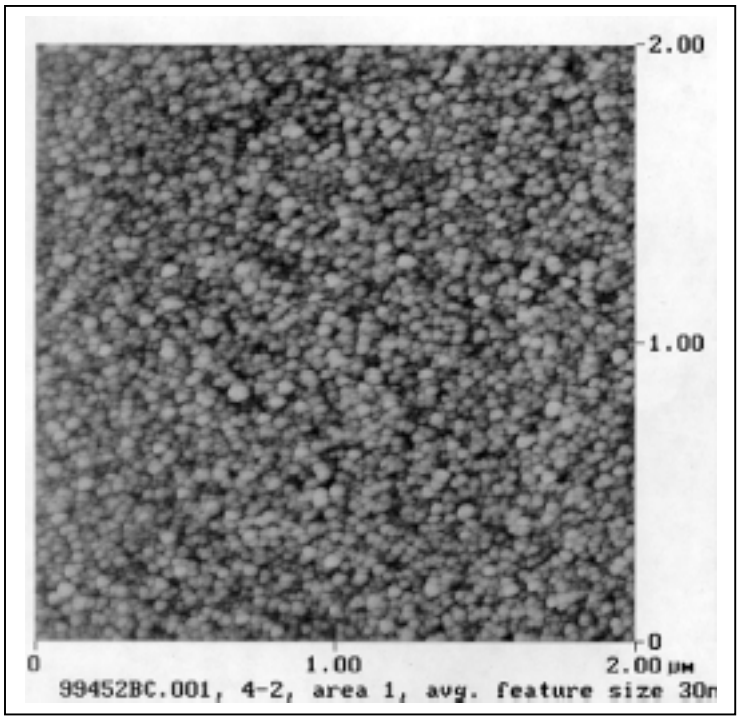


Figure 7. AFM image of the surface of a glass-ceramic substrate with an as-deposited barrier layer.

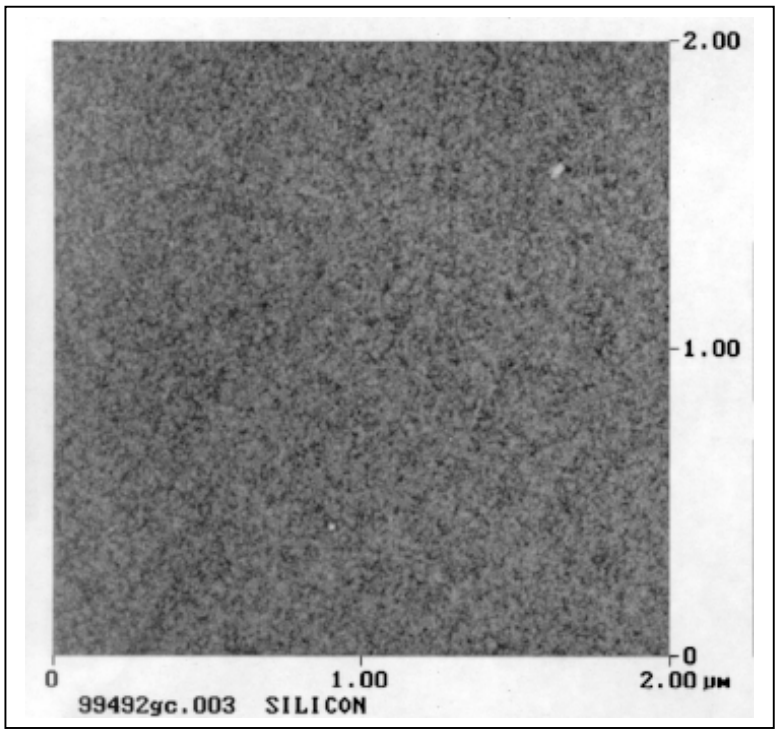


Figure 8. AFM image of the surface of the single crystal silicon reference.

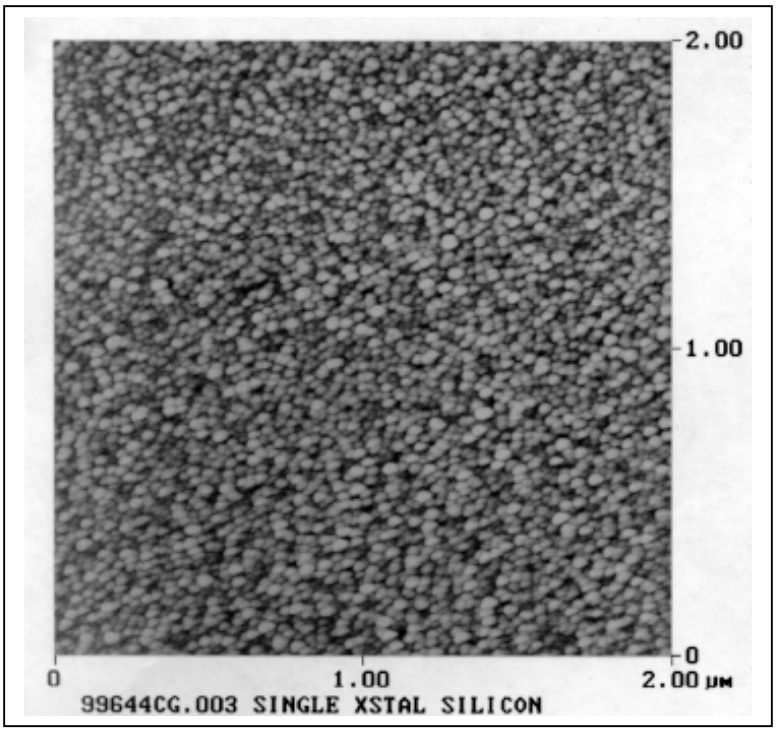


Figure 9. AFM image of the surface of the SiO_2/SiN_x barrier layer deposited onto the surface of the single crystal silicon reference and annealed at 900 ºC for 4 hours.

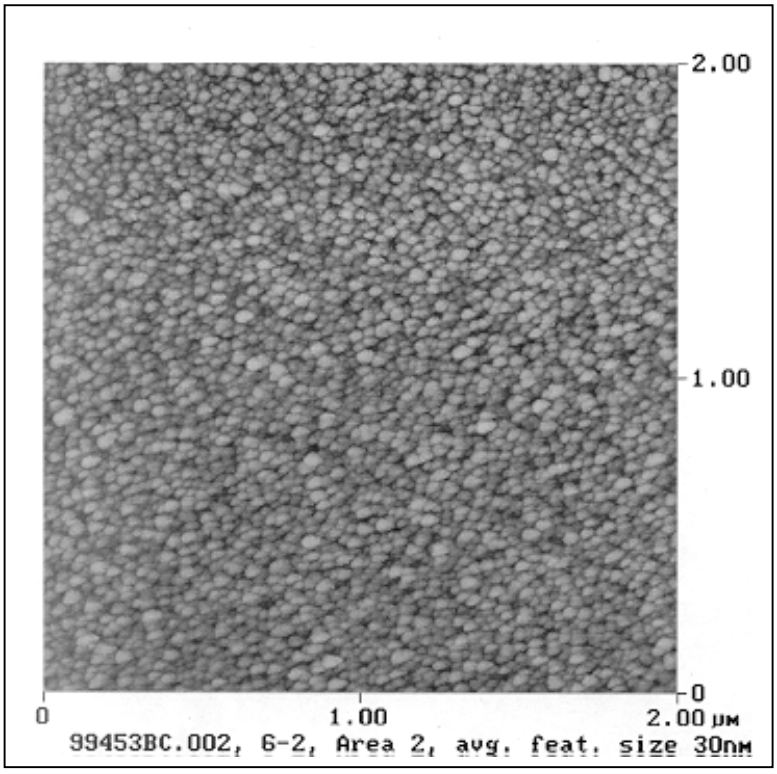


Figure 10. AFM image of a barrier layer coated glass-ceramic substrate annealed at 900 ºC for 4 hours in nitrogen.

This behavior is tentatively ascribed to the structural modifications of the barrier layer due to the thermal stress caused by the mismatch of the thermal expansion coefficients of the substrate ($2.6 \cdot 10^{-6}$ ºC^{-1}) and barrier layer ($0.5 \cdot 10^{-6}$ ºC^{-1} for SiO_2 and $2.5 \cdot 10^{-6}$ ºC^{-1} for Si_3N_4) during high temperature annealing.

- Optical transparency

Highly transparent glass substrates are required for thin film photovoltaic applications where the substrate is used as a cover glass (so called 'superstrate' cells). For this reason, optical transmission measurements were performed to determine the optical transparency of the glass-ceramic substrate. 1 mm thick glass-ceramic wafers were measured before and after they were coated with a PECVD barrier layer. As shown in the **Figure 11** the optical transparency of the glass-ceramics remains greater than 95% in the visible range after being coated with a PECVD barrier layer.

An interesting properties of glass ceramics (not investigated in this contract) is that the amount and even the directionality of light scattering in the superstrate can be tuned rather easily. Increasing the grain size from 10-15 nm to larger values, and selecting crystals more mismatched in the refractive index to the matrix will increase scattering in the superstrate. This feature is of interest in the thin film silicon solar cells as it increases the absorption length to a value larger than the film thickness.

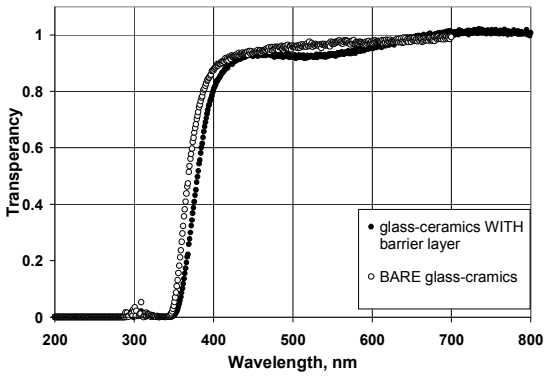


Figure 11. Optical transmission spectra of bare and barrier layer coated 1 mm thick glass-ceramic wafers.

3. Thin film transistors

- Fabrication

SIMS analysis of barrier layers is useful but only sensitive to impurities present in concentration greater than about 10^{16} cm^{-3}. It is well established that concentration of impurities as low as 10^{12} cm^{-3} can be detrimental to solar cell performance. To confirm the effectiveness of the new barrier layer, therefore, it is necessary to fabricate devices. The first devices fabricated were thin film transistors (TFTs). TFTs (**Figure 12**) are majority carrier devices, whose characteristics are very sensitive to mobile ions and the structure of polysilicon film. In particular, by analyzing the device, the density of defect related states in the bandgap of the deposited polysilicon film can be quantitatively measured.

To evaluate various barrier layer and substrate combinations, TFTs were fabricated on thermally oxidized silicon (860 nm), polished fused silica, PECVD barrier layer coated fused silica and PECVD barrier layer coated glass-ceramic wafers. The fabrication process started with depositing 100 nm thick amorphous silicon at 550 ºC by LPCVD using SiH_4/H_2 mixture. The TFT channel with the source and drain contact pads was formed by photolithography, followed by the deposition of the gate oxide (usually 100 nm) by LPCVD from the mixture of diethylsilane and oxygen at 450 ºC. The Poly-Si gate was deposited at 620 °C in LPCVD reactor and patterned by photolithography. Self-aligned ion implantation of phosphorus was conducted at ion energy of 100 kV to a dose of $10^{16}cm^{-2}$ using polysilicon gate as an implantation mask. After the ion implantation a 400 nm capping oxide was deposited by LPCVD and the wafers were subjected to a 4-hour anneal in nitrogen at 900 ºC in order to recrystallize the channel silicon and simultaneously activate implanted dopants. To complete the fabrication process another photolithography was performed to open contact windows in the capping oxide. A 250 nm thick aluminum film was deposited by evaporation and metal contacts were defined by lift-off technique. To reduce series resistance the contacts were later annealed at 400°C for 30 min in hydrogen ambient.

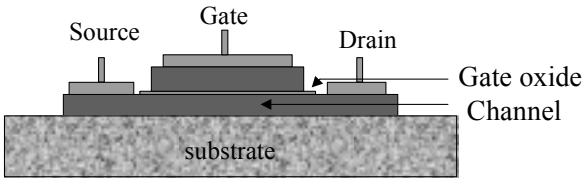


Figure 12. Schematics of a thin film transistor.

- Device Characteristics

Typical I-V characteristics of two different sets of transistors fabricated, one with a gate oxide thickness of 100 nm and another with 200 nm, are shown in **Figure 13** and the parameters extracted are listed in Table 2. Devices using either 100 nm or 200 nm gate oxide on either fused silica or glass-ceramic substrates had low leakage currents and exhibited a high carrier mobility. The 200 nm devices demonstrated electron mobility over 100 $cm^2/V{\cdot}sec$, but required high gate voltages (>40 V, as expected in a thick gate oxide device) to turn on. When comparing these results to those obtained on oxidized silicon wafers, we began to notice that the low leakage currents and high carrier mobilities were always measured in devices fabricated substrates, glass-ceramic and fused silica, which shared the common property of being insulating. Since TFTs on fused silica and oxidized silicon wafers were both fabricated on a very clean SiO_2 surface, and since thermal mismatch effects are small in our micron size test devices, this observation raised the question if the conductivity of the substrate influenced the device fabrication and/or electrical characteristics. In the case of oxidized silicon, a conducting ground plane underlies the device. In fused silica this ground plane is absent. The presence of the ground plane, in turn, influences the distribution of the electric field in the device. In the following, we will refer to this influence of the substrate as the 'conducting substrate model'. The alternative possibility is that the surface of fused silica differs sufficiently from that of thermal silicon dioxide to change the structure of the polysilicon deposited. We will term this model the oxide surface model.

To see which if these models were correct, we prepared a partly conducting, partly non-conducting substrate with a uniform surface of SiO_2. To do so, one half of a fused silica wafer was first coated with 1000 Å of highly conductive, heavily n^+ doped polysilicon deposited at 620 ºC by LPCVD (**Figure 14**). To insure a uniform SiO_2 surface, the whole wafer was then covered with a thin (2000 Å) PECVD silicon dioxide layer deposited at 245 ºC. As a result one half of the wafer was a bulk insulator, while the other half contained a conductive layer beneath a thin surface layer of SiO_2. Otherwise, the surface was the same in both halves, as was the CTE (coefficient of thermal expansion) as the later is controlled by the bulk of the substrate.

Thin film transistors were then fabricated on both halves. To contact the conductive layer, we opened a window in the top oxide. This permitted us to apply a known voltage to the polysilicon. Electrically, the buried polysilicon layer functions as second or "back" gate. The I-V characteristics of the various TFTs were then measured at a series of fixed back gate voltage. TFTs fabricated on the non-conducting half of the wafer were used as reference.

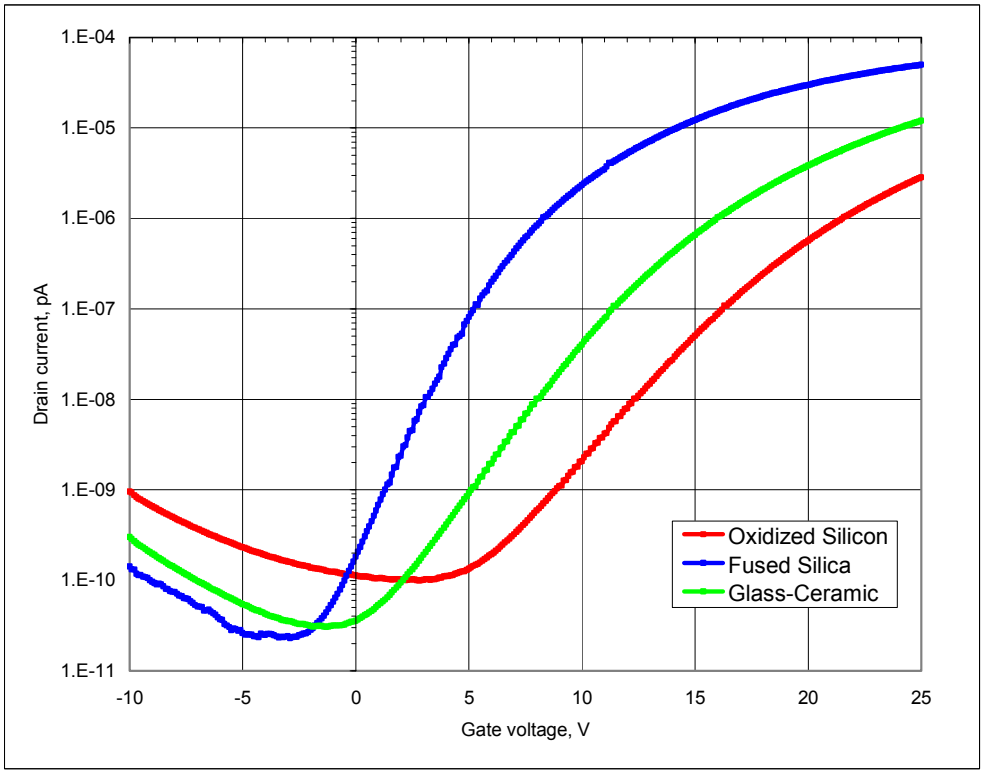


Figure 13. Current-Voltage characteristics of TFTs fabricated on oxidized silicon, fused silica and glass-ceramic substrates.

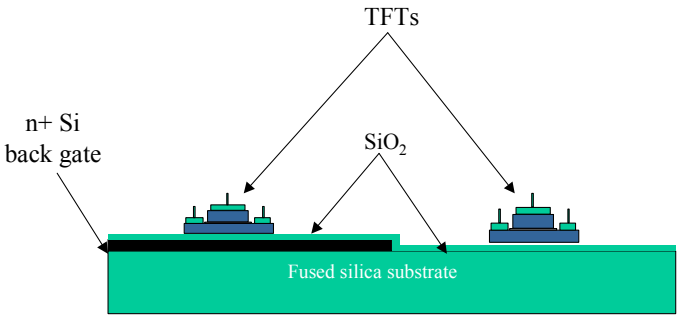


Figure 14. Design of the test TFT series (a) fabricated on fused silica substrate with conducting layer (back gate).

Table 2. Parameters of TFTs fabricated on glass-ceramic, fused silica and oxidized silicon wafers. The columns list, left to right, the flat band voltage, V_{fb}; the leakage current, I_{min}, in pA; the source-drain current at zero gate voltage, I_0, in pA; the source-drain current at gate voltage of 15 V, I_{15}, in pA; the intrinsic electron mobility μ in $cm^2/V{\cdot}sec$; the trap density Q_{trap} in multiples of $10^{12}/cm^2$; the subthreshold swing S in V/decade; and the threshold voltage V_{th}. The line below lists the standard deviations of these parameters.

	V_{fb}	I_{min}	I_0	I_{15}	μ	Q_{trap}	S	V_{th}
Si 100 nm gate oxide	2.7	83	99	63499	36.70	6.71	3.41	15.4
	0.7	14	17	48061	8.97	0.37	0.26	1.3
fused silica 100 nm gate oxide	-4.3	13	1125	3494438 6	80.24	4.90	1.29	3.3
	0.4	4	3043	491092 3	9.10	0.18	0.11	0.5
Glass-ceramic 100 nm gate oxide	-0.8	25	26	260110	66.19	7.10	3.08	13.0
	0.7	4	4	148557	14.90	0.28	0.22	0.8
coated fused silica 100 nm gate oxide	-2.2	38	196	121204 72	39.25	4.81	1.68	5.8
	0.3	4	95	395187 3	3.15	0.29	0.14	1.0
Si 200 nm gate oxide	5.3	129	153	1145	54.66	6.18	5.57	26.9
	1.4	32	42	1037	11.16	0.15	0.51	2.0
fused silica 200 nm gate oxide	-0.1	29	29	721	46.44	7.22	5.98	28.0
	0.8	3	3	152	12.51	0.15	0.24	0.5
Glass-ceramic 200 nm gate oxide	-2.6	27	36	57402	112.28	6.04	4.07	18.4
	0.9	5	19	77945	22.49	0.36	0.37	2.3
coated fused silica 200 nm gate oxide	-3.8	35	55	92057	101.95	5.92	4.28	16.5
	0.4	4	10	77352	39.09	0.36	0.52	1.5

The electric characteristics of the TFTs made on the two halves of this special wafer were found to be similar to those obtained on separate fused silica and oxidized silicon substrates (**Figures 13 and 15**). TFTs on the substrate section with an underlying conductive layer had higher leakage currents than those fabricated without it. When no voltage was applied to the back gate ("floating back gate"), the TFT performance was poor and the TFT parameters were unstable. We also observed that the leakage current and flat band voltage depended on the measurement history indicating the trapping of electric charge at the back interface. Applying voltage to the back gate stabilized the TFT parameters and permitted to control the leakage current hence to minimize it. I.e., the source-drain current could be controlled with the back gate as well as with the top one. **Figure 16** shows the I-V curves of a transistor with the a) drain current controlled by the top gate with a fixed voltage known as the flat band voltage applied to the back and b) controlled by the back gate with a fixed voltage applied to the top gate. The difference in

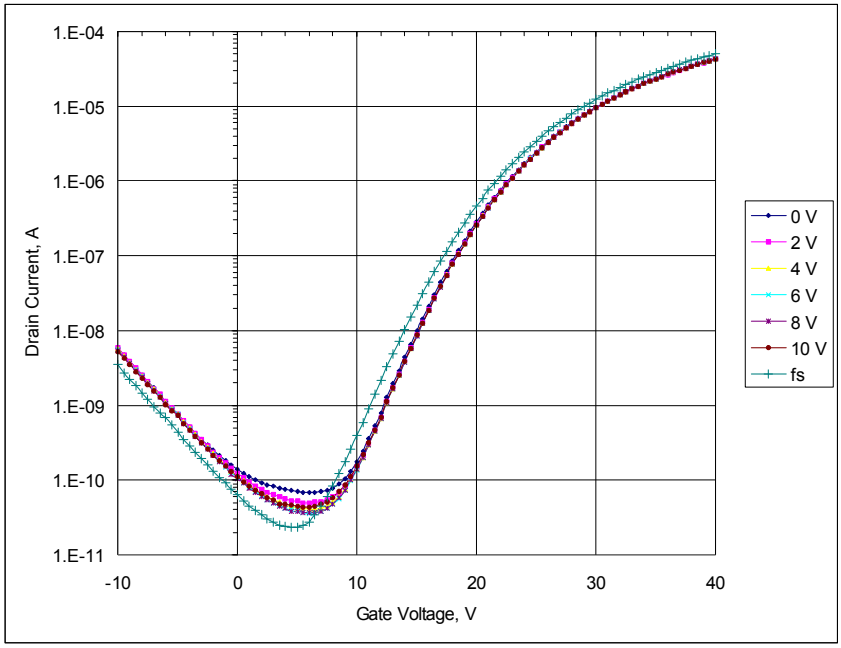


Figure 15. Current-voltage characteristics of TFTs fabricated on fused silica substrate with conducting layer (back gate). Drain current was measured as a function of top gate voltage at various fixed back gate voltages (denoted 0V, 2V, 4V, 6V, 8V and 10 V). 'fs' denotes the curve measured in the device fabricated on the section of the substrate with no back gate (thick insulator).

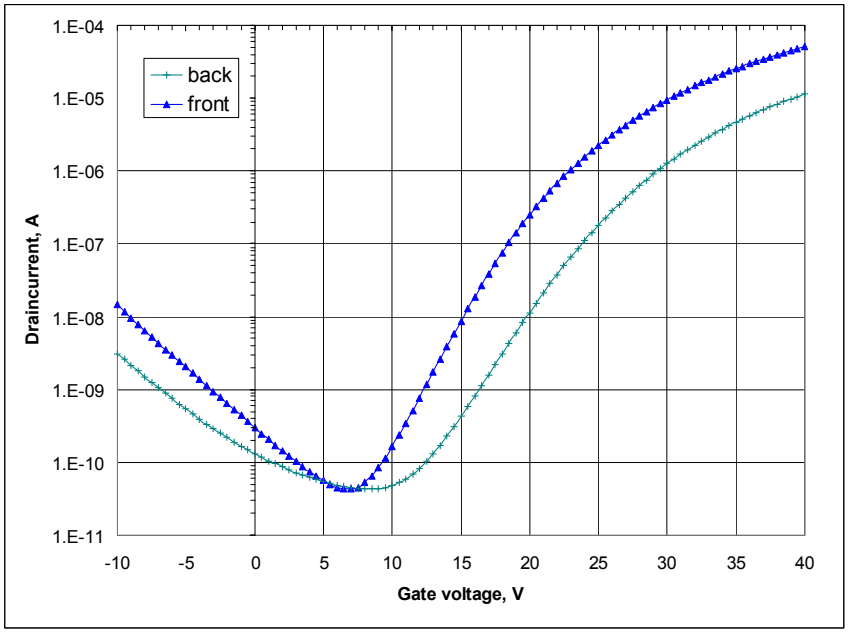


Figure 16. Current-Voltage characteristics of TFT controlled by the top gate with the back gates at fixed potential equal to the flat-band voltage of 8 V ("front"), and by the back gate with the top gate at fixed voltage of 7 V ("back").

the drain current at a given gate voltage reflects the different effective gate size, gate oxide properties and thickness as well as the different structure of the channel polysilicon at the top and bottom oxide interface.

The fact that leakage currents of the TFTs with back gates still exceeded those of reference devices fabricated on bulk insulating section (**Figure 15**) indicates that details of the electric field distribution, especially at the drain end, are important.

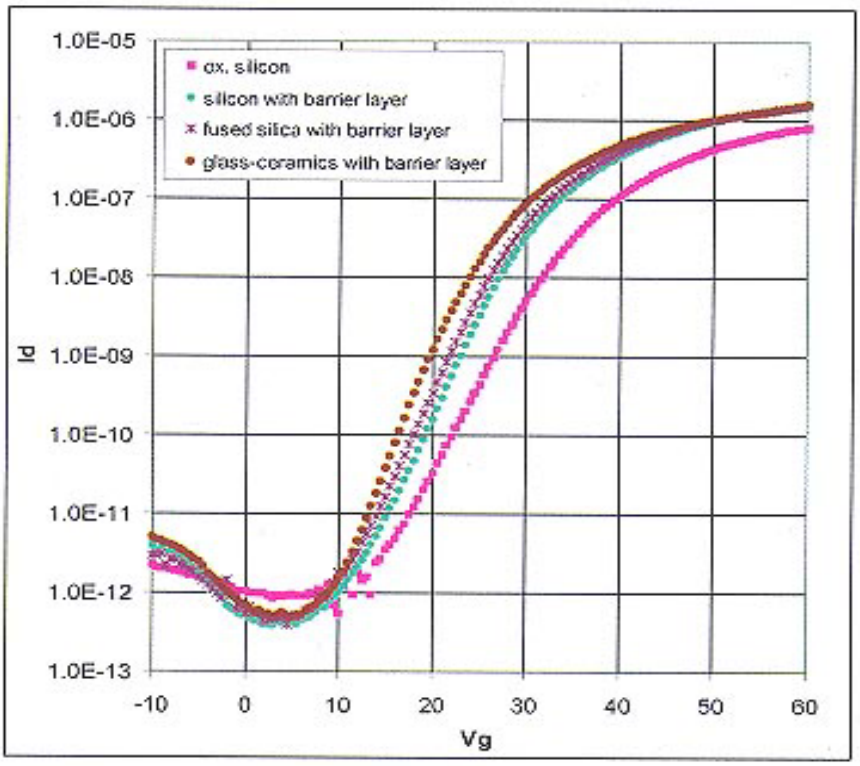
- Density of polysilicon mid-gap states before and after hydrogenation

To study the influence of the substrate surface on the structure and electric properties of polysilicon films, we analyzed the temperature dependence of the source drain current at various gate voltages. This procedure permits to measure the density of gap states (DOS) of polysilicon films deposited on different substrates. The activation energy of conduction provides information on the position of the Fermi level, which, when combined with analysis of the charge required to move Fermi level incrementally, permits to derive quantitative values for DOS as the Fermi level is moved through the gap.

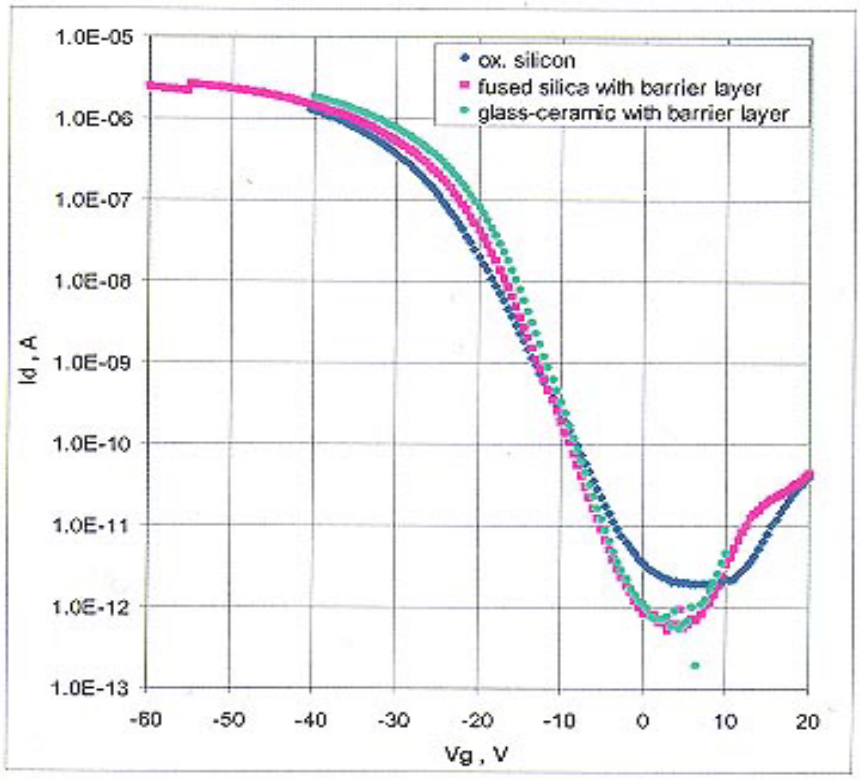
To map the DOS above and below the Fermi level, we fabricated and measured both n- and p- channel transistors. Devices with a 100 nm thick low temperature gate oxide were fabricated on barrier layer coated glass-ceramic, fused silica and oxidized silicon substrates. Typical I-V characteristics of these TFTs measured at room temperature are shown in **Figure 17**. To map the DOS, the drain current I_d was measured versus gate voltage V_g at fixed source-drain voltage V_{sd} in the temperature range 293 – 423 K (**Figure 18**). The activation energy E_a of conductivity was extracted and its dependence on gate voltage (**Figure 19**) was analyzed using the procedure in reference [7] to derive the DOS.

Figure 20 shows the DOS plots of polysilicon films deposited on different substrates. The near mid-gap DOS of as-deposited films is very high ($\sim 10^{19}$ $cm^{-3}eV^{-1}$) and very similar on all substrates types, to the point where the various curves are difficult to distinguish from each other.

To improve the performance of the TFTs fabricated, and to advance the DOS method we hydrogenated our transistors in an ECR hydrogen plasma at 360 °C for 2 hours and then re-measured the devices using a narrow temperature interval to avoid 'dehydrogenation' of the device during the measurement. **Figure 21** shows I-V curves measured before and after hydrogenation of n-channel TFTs fabricated on oxidized silicon, barrier layer coated glass-ceramic and fused silica substrates. As can be seen from **Figure 21,** the characteristics of the TFTs improved significantly after hydrogenation. The steeper subthreshold slopes indicate improved carrier mobility and a lower density of mid-gap states. Hydrogenation is known to passivate electrically active states deep states (most of which are associated with grain boundaries). In our devices, hydrogenation reduced the overall density of states by up to two orders of magnitude (**Figure 22b**). The lower DOS of these hydrogenated polysilicon films now permits to see more clearly small difference in the DOS deposited on different substrates. The films deposited on the very smooth surface of oxidized silicon exhibit the lowest DOS value ($\sim 10^{17}$ $cm^{-3}eV^{-1}$). At the same time DOS of the films deposited on the barrier layer coated glass-ceramic and fused silica substrates are about an order of magnitude higher. To verify the hypothesis, that the surface roughness influenced the DOS of the deposited

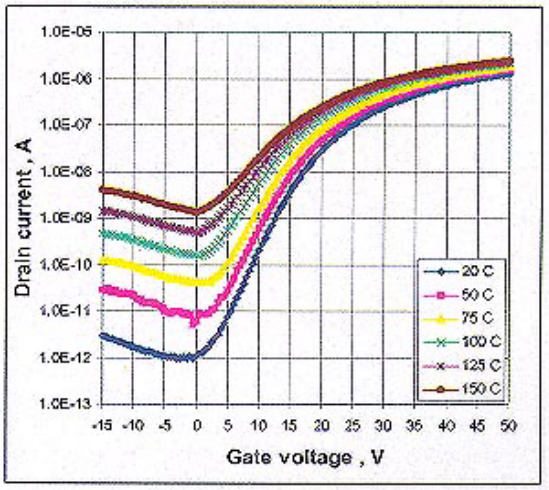


(a)

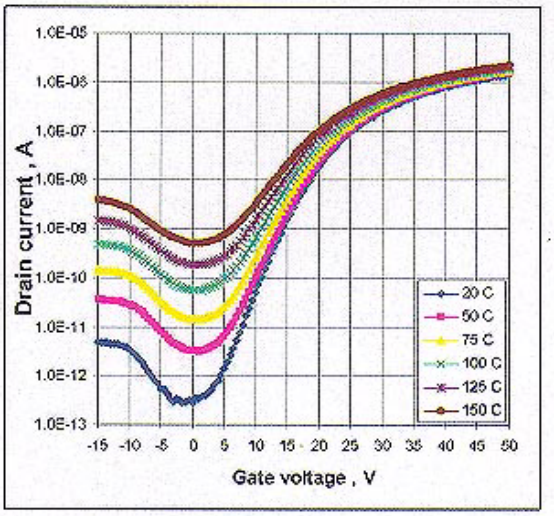


(b)

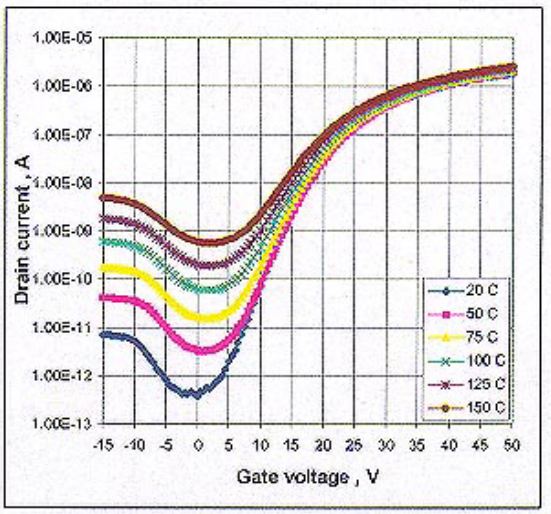
Figure 17. Transfer characteristics of n- channel (a) and p- channel (b) transistors fabricated on oxidized silicon, barrier layer coated fused silica and glass-ceramic substrates.



(a)



(b)



(c)

Figure 18. I-V curves measured at different temperatures on TFTs fabricated on oxidized silicon (a), glass-ceramic (b) and fused silica (c) substrates.

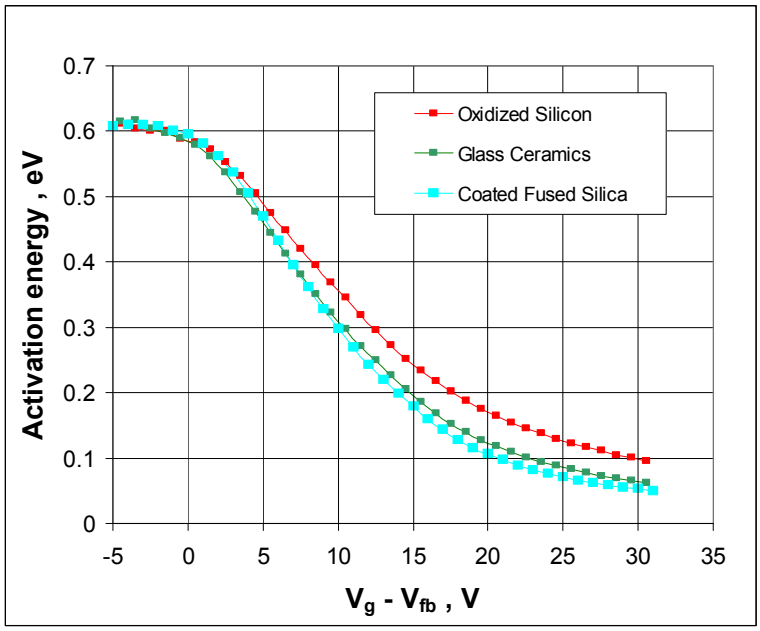


Figure 19. Dependence of the source-drain conductance activation energy on the gate voltage of TFTs fabricated on oxidized silicon, glass-ceramic and fused silica wafers.

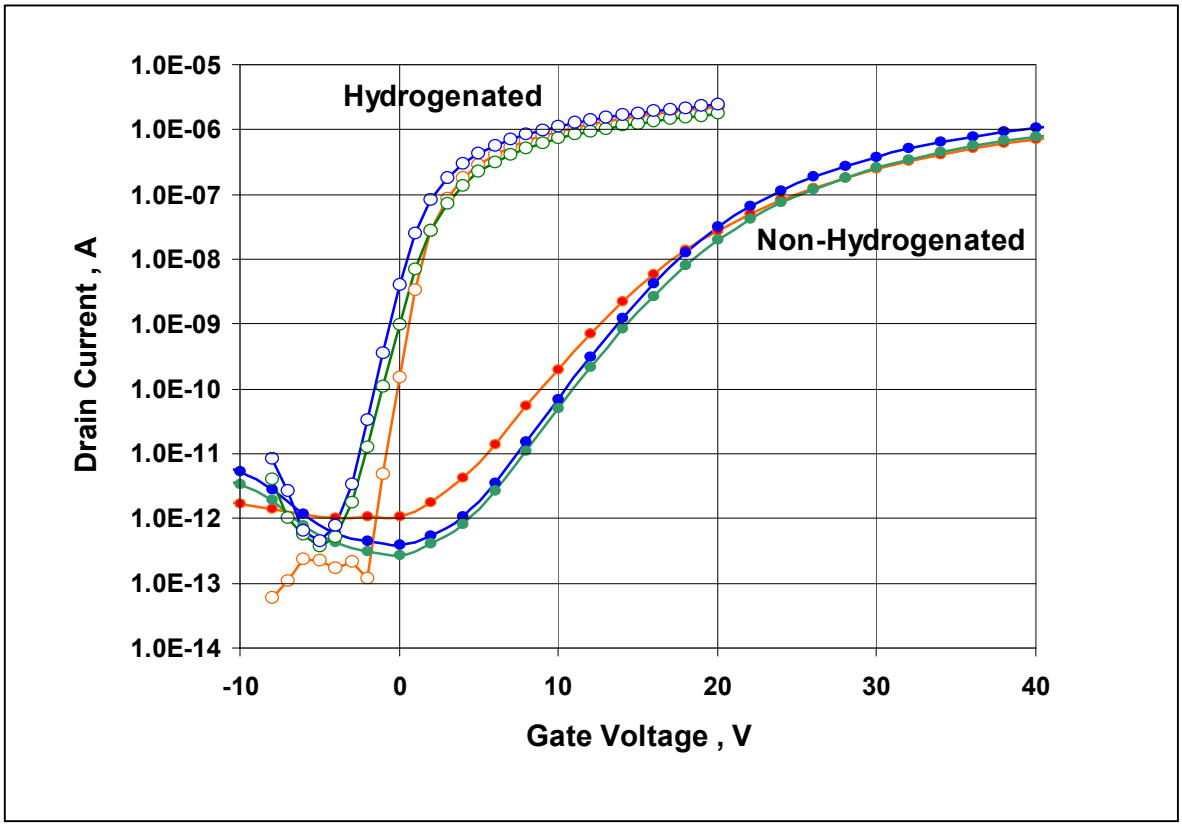


Figure 20. I-V characteristics of TFTs measured before and after hydrogenation. TFTs were fabricated on: oxidized silicon wafer - red curves; barrier layer coated glass-ceramics – green curves; barrier layer coated fused silica – blue curves.

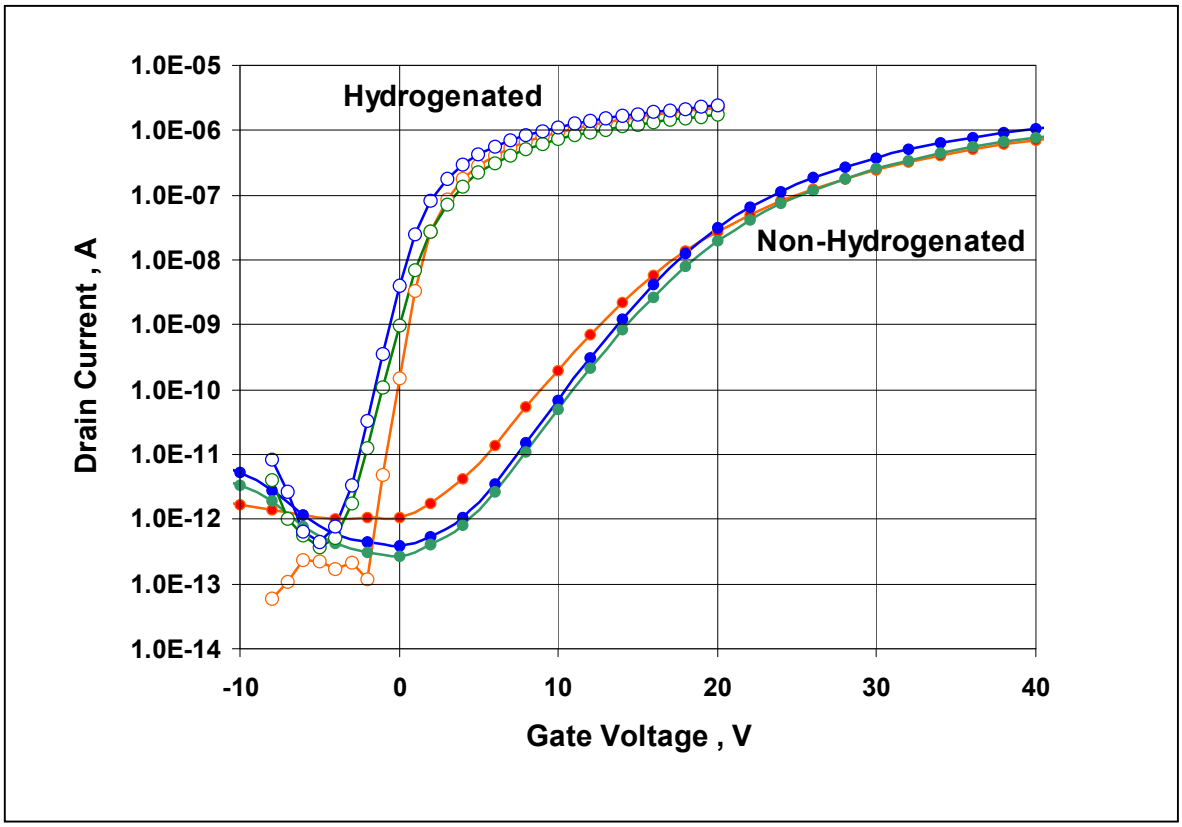
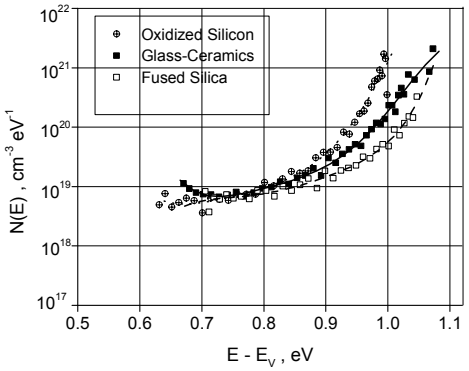


Figure 21. I-V characteristics of TFTs measured before and after hydrogenation. TFTs were fabricated on: oxidized silicon wafer - red curves; barrier layer coated glass-ceramics – green curves; barrier layer coated fused silica – blue curves.

silicon films, we analyzed films deposited on bare and barrier layer coated fused silica substrates. Using the same pure substrate, but changing its surface roughness by depositing an otherwise unnecessary barrier layer made it possible to separate the effect of surface roughness from the effect of impurity out-diffusion from the substrate, an effect that also can increase the DOS. Since the fused silica wafers we used are of high quality and could not act as source for impurities, the surface roughness was the only factor left to affect the DOS of the deposited films. **Figure 23** shows that the DOS of the film deposited on the smooth surface of bare fused silica are almost order of magnitude lower than that films deposited in the same run on barrier layer coated substrate.

(a)



(b)

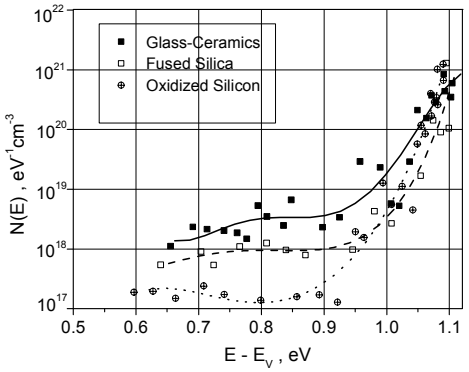


Figure 22. DOS of non-hydrogenated (a) and hydrogenated (b) polysilicon films deposited on oxidized silicon, barrier layer coated fused silica and glass-ceramic substrates.

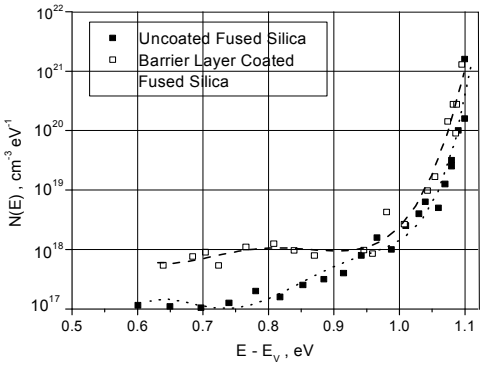


Figure 23. DOS of hydrogenated polysilicon films deposited on bare and barrier layer coated fused silica substrates.

- Bias Temperature Stress, BTS, tests

To validate our SIMS results indicating that no mobile ions diffuse through the barrier layer from the substrate into the deposited films, we carried out bias-temperature stress (BTS) tests. The BTS is a technique that characterizes the long-term stability of thin film transistors and MOS capacitors [8] and is much more sensitive than SIMS to presence of mobile ions reaching the gate oxide. The method is highly suitable to test the out-migration from the substrate since the substrate mainly is SiO_2 as is the gate dielectric. Impurities mobile in the substrate, if they reach the gate, are therefore also mobile in the gate and can be detected by drifting them in the gate field ($\sim 10^6$ V/cm). This drift, in turn, changes the capacitance-voltage relationship of the gate.

The C-V measurements were performed as follows. Both the source and drain of the thin film transistor was grounded and bias was applied to the gate. Typical C-V curves taken in BTS cycles are presented in **Figure 24a-c**. Devices on fused silica and glass-ceramics substrates were found to be very stable and reproducible with flat-band voltage shifts of less then +7 V when cycled at 200 ºC, + 50 V for 10 min (positive stress). The C-V curve returned to the initial flat band voltage after negative stress (-50 V, 200 ºC, 10 min.). On the other hand, devices on oxidized silicon substrates were found to be very unstable. The gate oxide, when tested at temperatures above 120 ºC, went "of scale" in less then a minute at the voltages employed to test the other devices. Therefore, the curves shown in **Figure 24c** were taken after stressing these devices at the lower temperature of 100 ºC and the shorter time of one minute, while keeping the applied voltage at 50 V. Note that after a positive stress the C-V curve moved left to a high negative flat band voltage. It was not possible to quantify this shift because the new flat band voltage exceeded our voltage sweep limit. After a negative stress, the C-V curve returned to the initial values of the flat band voltage. The electrical instability of the devices fabricated on oxidized silicon wafers, relative to those formed on fused silica and glass-ceramics, is linked to the 'floating gate' issue discussed above and can be avoided by fixing the electrical potential of the conducting substrate.

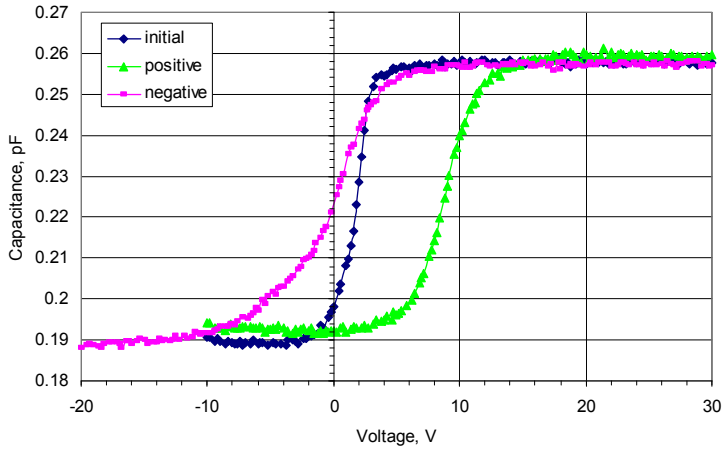
Overall, the results indicate that only insignificant amounts of mobile ions are present our TFTs. This observation supports our conclusion that surface roughness is the only major factor affecting the electronic structure of the investigated polysilicon films.

4. P-I-N diodes

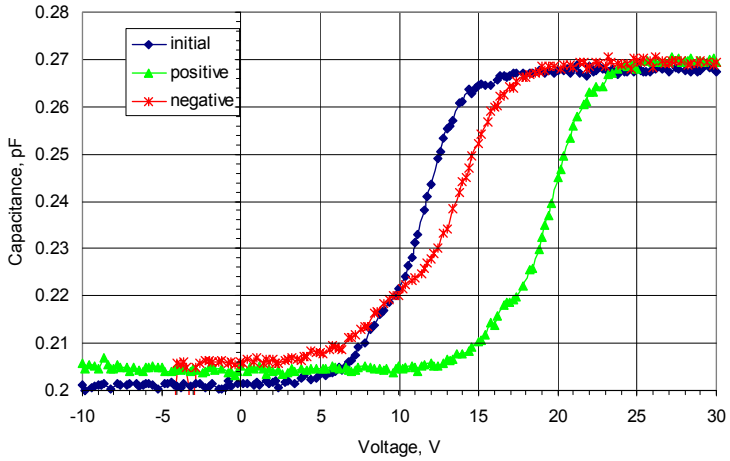
- Recrystallized polysilicon films

To investigate the effectiveness of the various barrier layers used to coat glass-ceramics and to demonstrate that properly barrier coated glass ceramic substrates can serve as substrates for manufacturing thin film solar cells we fabricated minority carrier devices, i.e. p-i-n junction diodes. These devices were made on glass-ceramic substrates coated with either the triple-stack LPCVD or the simpler 1000 Å SiN_x /1000 Å SiO_2 PECVD barrier layer. Control wafers of oxidized silicon and fused silica (bare and coated with the above barrier layers) were processed along with the glass-ceramic substrates. Oxidized silicon wafers, unlike the other two substrate types, are not transparent and for this reason, cells made on silicon substrates could not be illuminated from the backside.

a.



b.



c.

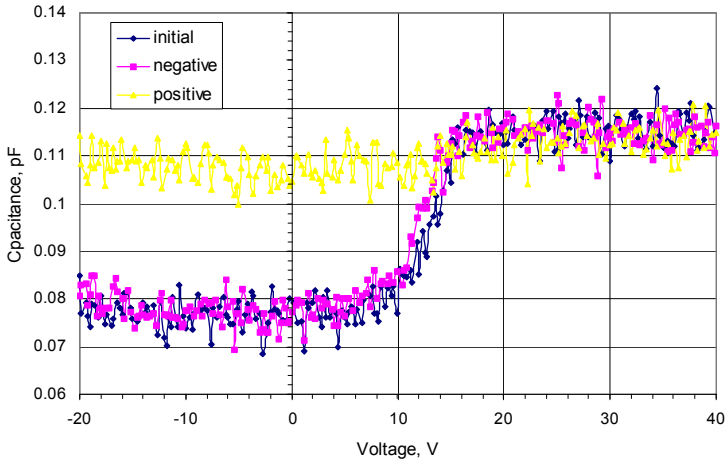


Figure 24. C-V curves of TFTs measured before and after positive and negative Bias Temperature Stress tests. a. – fused silica substrate, 200 ºC, 50 V, 100 min.; b. – glass-ceramic substrate, 200 ºC, 50 V, 10 min.; c. – oxidized silicon substrate, 100 ºC, 50 V, 1 min..

Because the use of a top Al contact (see below) the cells could not be illuminated from the top side either. The cell characteristics under illumination thus could not be compared to cell fabricated on glass or glass-ceramic substrates. The lack of transparency reduced the usefulness of solar cells on oxidized silicon as a 'standard'; however, these cells can still compared to precisely to our other cells in their dark I-V characteristics. Such measurements provided useful insights, see below.

The fabrication process started with the Low Pressure Chemical Vapor Deposition (LPCVD) of 500 Å n+, 6000 Å undoped (i-) and 1500 Å p+ polysilicon layers at a temperature 550 °C followed by a 4 hour anneal at 900 °C. These process parameters were chosen based on previous experiments to optimize the quality of polysilicon films for thin film transistors. The structures were then patterned by photolithography and chemically etched to form isolated devices. Aluminum contacts were deposited on the top to increase the reflectance from the backside and to enhance effective light absorption. The contacts were annealed in hydrogen at 400 ºC for 0.5 hour to enhance the contact adhesion and decrease series resistance.

The dark current-voltage characteristics (I-V) of both solar cells and p-i-n junction diodes were measured and analyzed. All devices on glass-ceramic substrates coated with the PECVD barrier layer exhibited reverse leakage currents similar to those fabricated on oxidized silicon wafers and compared to devices fabricated on the physically much rougher original triple LPCVD barrier layer, had approximately a 100 times lower reverse leakage current at –1 V. This finding, again, indicates that a low surface roughness of the barrier layer is important (**Figure 25**). Control solar cells fabricated on fused silica substrates (both bare and coated) had very high leakage currents.

Inspection of the surface of the polysilicon films with an optical microscope showed that films deposited on fused silica substrates had long (millimeters) and wide (tens of microns) cracks (**Figure 26**). Even traces of polysilicon film exfoliation were detected. The cracks are caused by the difference of the thermal expansion coefficients of polysilicon and fused silica. During cooldown from the high temperature anneal (900 ºC, 4 hours) the difference in CTE induces a tensile strain of 0.2% into the polysilicon film. The corresponding tensile stress, therefore, reaches 60 000 psi, this value exceeds the breaking strength of polysilicon, which is between 10 000 and 35 000 psi [9]. Inspection also showed that the cracks propagated into to the out-diffusion barrier layer. The presence of these cracks explains the poor quality of solar cells and minority carrier devices fabricated on fused silica substrates.

This result indicate that while the CTE matched glass-ceramics and silicon substrates permit to deposit the thick films required for solar cell fabrication without introducing undue "thermal" stress, fused silica is not a suitable substrate for thin film solar cells fabricated at high temperatures.

- Directly deposited polysilicon films

To accelerate the solar cells fabrication, we changed our process, from amorphous silicon deposition followed by recrystallization, to the direct deposition of polysilicon. The reason for this is that the LPCVD deposition of amorphous silicon from silane at 550 ºC is slow (20 Å/min), limiting a typical run to less than 1 micron. The higher deposition

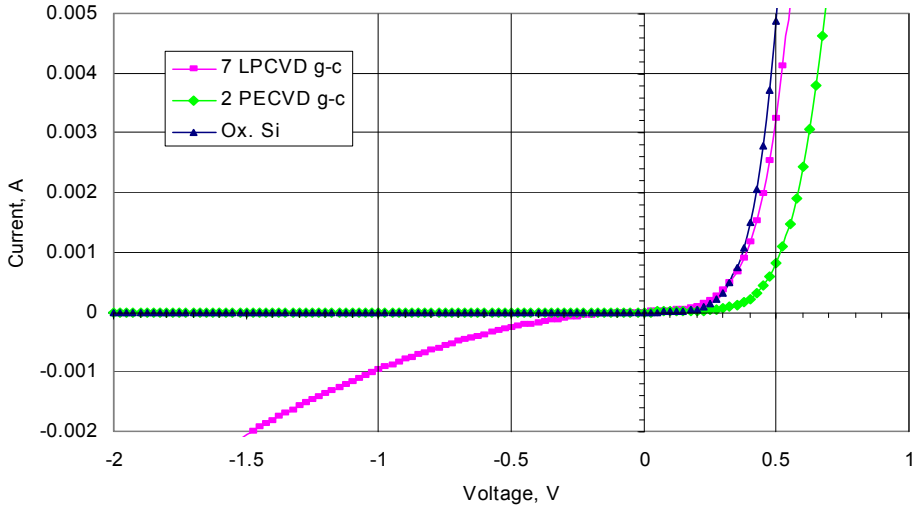


Figure 25. Dark current voltage characteristics (I-V) of p-i-n junction diode fabricated on oxidized silicon substrate and glass-ceramic substrates coated with different barrier layers. (7 LPCVD g-c denotes a device on a triple LPCVD SiN_x/SiO_2 barrier layer coated glass-ceramic; 2 PECVD denotes a device on a single PECVD SiN_x/SiO_2 barrier layer coated glass-ceramic; Ox. Si denotes a device on an oxidized silicon substrate).

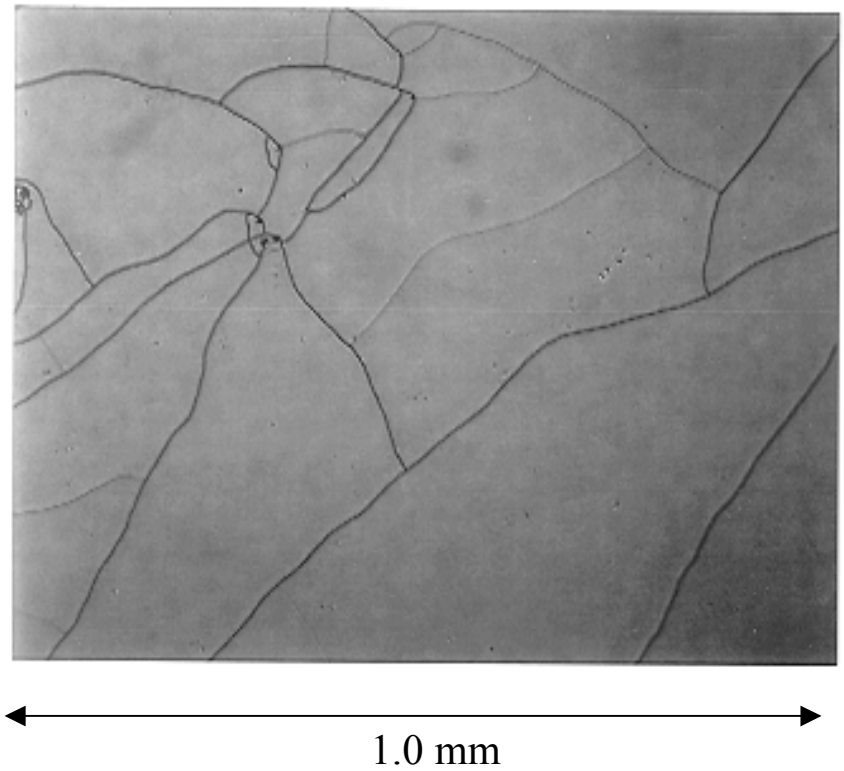


Figure 26. Optical image of cracked polysilicon film processed on fused silica substrate.

rate of 600 Å/min at 700 ºC allowed depositing in reasonable time the thicker films needed to more effectively absorb light in solar cells.

A series of solar cells and minority carrier devices using polysilicon deposited at 700 ºC was fabricated on glass-ceramic, oxidized silicon and fused silica substrates. In this initial run, the thickness of the polysilicon film was chosen to be the same as in the previous series (below 1000 nm) to facilitate comparison. The dark I-V characteristics were measured and analyzed. **Figure 27** shows the results for devices on glass-ceramic substrates. It was found that the new deposition process increased the reverse dark current of solar cells on both glass-ceramic and oxidized silicon substrate up to 20 times.

The reason for the poorer performance of devices fabricated at higher temperature was found in a difference of a processing parameter (namely etching) of the films deposited at these temperatures. It is known that at the temperatures higher than about 580ºC silicon film is deposited in the polycrystalline form while at 550 ºC its amorphous. The important difference is that the solar cell process requires now to pattern polycrystalline (rather then amorphous) silicon. Because of the presence of grain boundaries the etching behavior of polysilicon in liquid etchants is distinctively different from that of amorphous silicon.

To advance the fabrication process we first fabricated a set of devices where polysilicon film was patterned with wet etching using a photoresist mask. Electrical testing showed that most of the junctions were shortened and the devices did not work as diodes. Visual inspection revealed numerous defects in the i-layer at the edges of the devices (**Figure 28a**). These defects created conducting bridges between n- and p- layers that caused the device to fail. The defects were suspected to form due to the higher etching rate along grain boundaries during the wet etching of the i-layer.

We developed a special recipe for dry reactive ion etching (RIE) that yielded structures etched controllably with a high aspect ration. A layer of patterned 500 nm thick

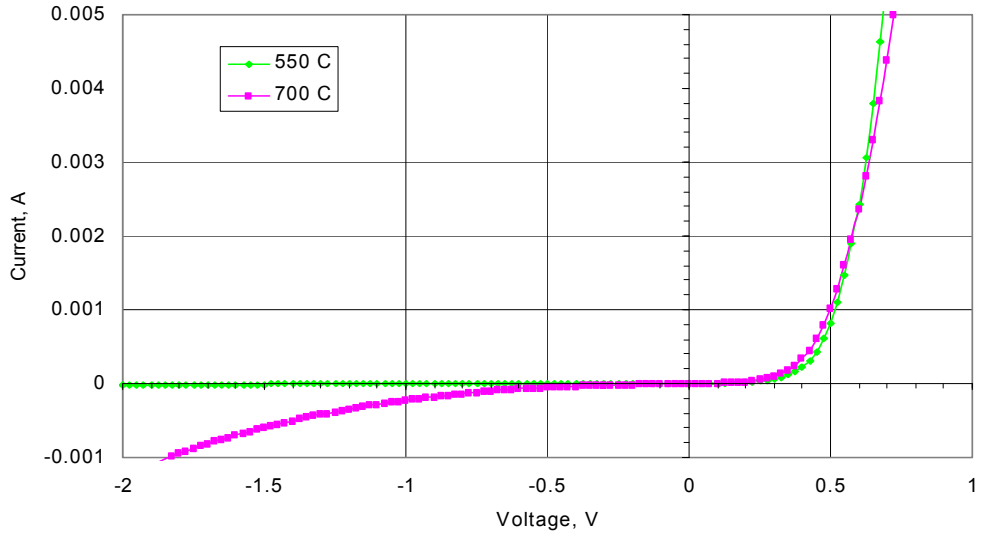


Figure 27. Dark current voltage characteristics (I-V) of p-i-n junction diode fabricated on glass-ceramic substrate coated with PECVD SiN_x/SiO_2 barrier layer, using polysilicon deposited at 550 ºC and recrystallized at 900 ºC (denoted 550 C) and polysilicon deposited directly at 700 ºC and annealed at 900 ºC (denoted 700 C)

LPCVD SiO_2 was used as an etching mask. Optical microscopy images show that RIE patterning of polysilicon film using a silicon dioxide mask produced features with a more sharp and accurate edge. This is illustrates in **Figures 28c** and **28b** showing a dry-etched film and a wet etched film both using SiO2 as an etch mask. The high aspect ratio of the etching became even more important we started working with thicker (over 1 micron thick) films.

Fabrication of the high efficiency, multilayer thin film solar cell proposed by Martin Green [10] requires the deposition of multiple p-i-n structure. This structure forms a rectifying electrical junction, the properties of which determine the effectiveness and quality of the solar cell. The intrinsic (i-) polysilicon layer is required for effective light absorption and separation of generated charge carriers. The parameters of this layer are crucial for operation of the solar cell.

We started this investigation by studying the fabrication of high quality p^+-i-n^+ junctions. To optimize their performance we fabricated four runs of p^+-i-n^+ diodes, where stacks of in-situ doped p^+, n^+ and undoped (i) polysilicon films were directly deposited at 620 ºC on barrier layer coated glass-ceramics and control oxidized silicon wafers (**Figure 29a,b**). The films were patterned by photolithography and etched using developed RIE process. Various temperature treatments were investigated to optimize dopant activation. Al contacts were deposited on the top and annealed in hydrogen.

The fabricated diodes included both junctions employing a direct p^+-n^+ contact as well as p^+-i-n^+ structures. The reason for inserting a thin (20 nm) i-layer was to lower the susceptibility of junctions to the tunnel breakdown which otherwise occurs at low voltages between the highly doped p^+ and n^+ regions.

The dark I-V characteristics of the diodes were measured and analyzed. It was found that films deposited at 620 ºC and annealed at 900 ºC formed the best junctions with rectifying ratios over 10^5 at 1 V (**Figure 30**). Insertion of a thin i-layer significantly increased the leakage current (up to 3 orders of magnitude) and lowered the slope of the forward I-V curve (**Figure 31**). This phenomenon can be explained by considering that a thin layer of undoped silicon does not significantly change the width of the depleted region, but does act as a source of defects forming additional generation-recombination states in the gap. Presence of these centers, in turn, degrades the performance of the diodes. No sign of tunnel breakdown was found at reverse voltage up to as high as 5 V.

The high series resistance of the junctions limiting the forward current at voltages higher than 0.6 V is due to relatively high sheet resistance of the films and can be reduced by optimizing the design of the diodes.

To optimize the parameters of the p-i-n junctions we fabricated a series of the diodes varying the thickness of the i- layer from 100nm to 2000 nm. The fabrication process was similar to that described above where p-i-n polysilicon stacks were directly deposited in LPCVD furnace at 620 ºC on and then annealed at 900 ºC in nitrogen to activate the dopants.

The dark I-V characteristics of the fabricated diodes were measured and analyzed. **Figure 32** shows typical I-V curves of the devices fabricated oxidized silicon wafers. The thickness of the i- layer is 180 nm, 540 nm, 1200 nm and 1900 nm. For comparison analysis, we used rectifying ratio R of the diodes at fixed bios (0.6 V) as a characterizing parameter.

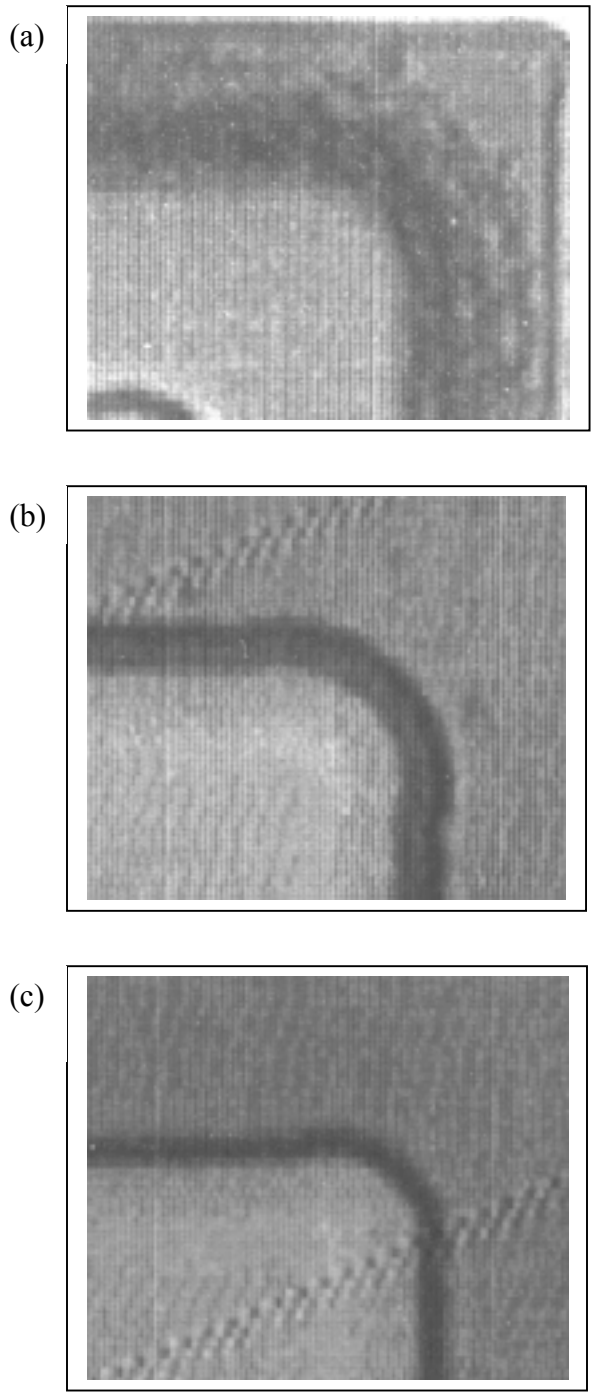


Figure 28. Optical microscopy images of polysilicon films patterned using: (a) wet etched, photoresist mask; (b) wet etched, SiO_2 mask; (c) RIE, SiO_2 mask.

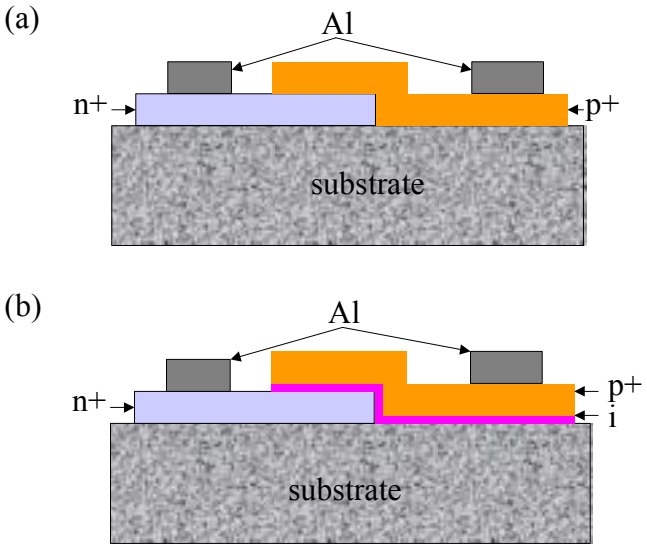


Figure 29. Schematic cross-section of p^+-n^+ (a) and p^+-i-n^+ (b) diodes.

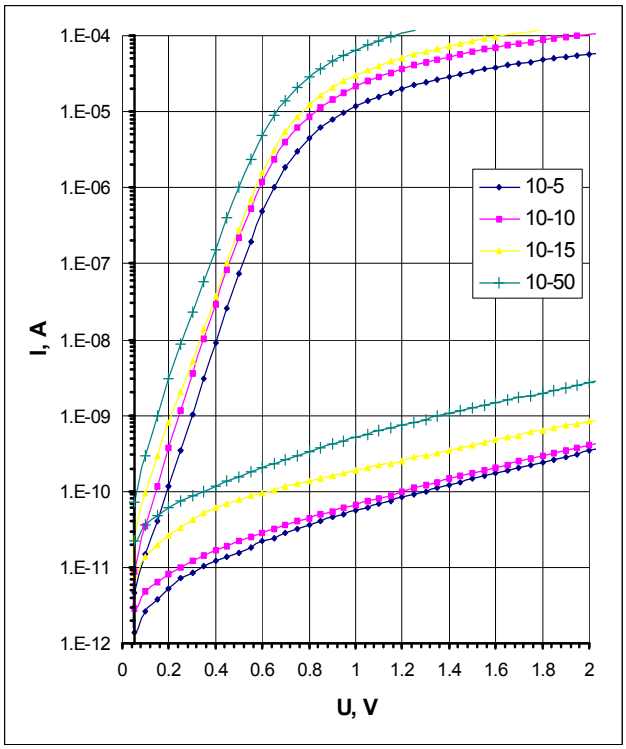


Figure 30. Dark I-V characteristics of p+-n+ diodes. Junction size: 10x5 microns (denoted 10-5), 10x10 microns (denoted 10-10), 10x15 microns (denoted 10-15), 10x50 microns (denoted 10-0).

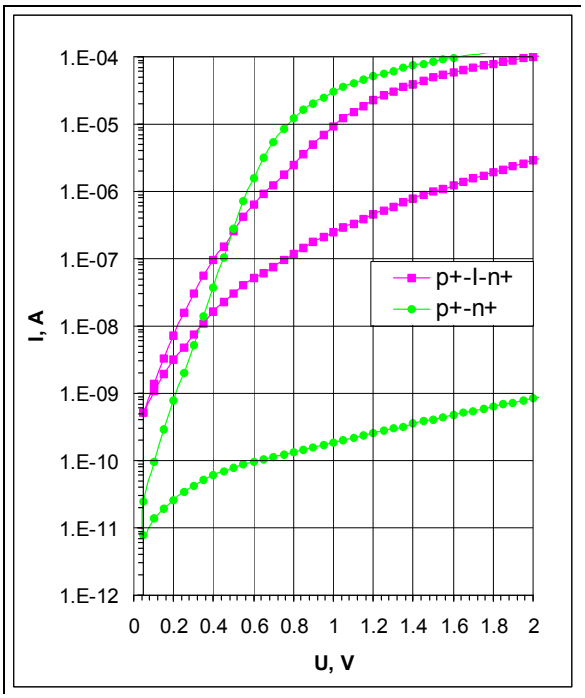


Figure 31. Dark I-V characteristics of p^+-n^+ (green) and p^+-i-n^+ (red) diodes. Thickness of i-layer is 20 nm.

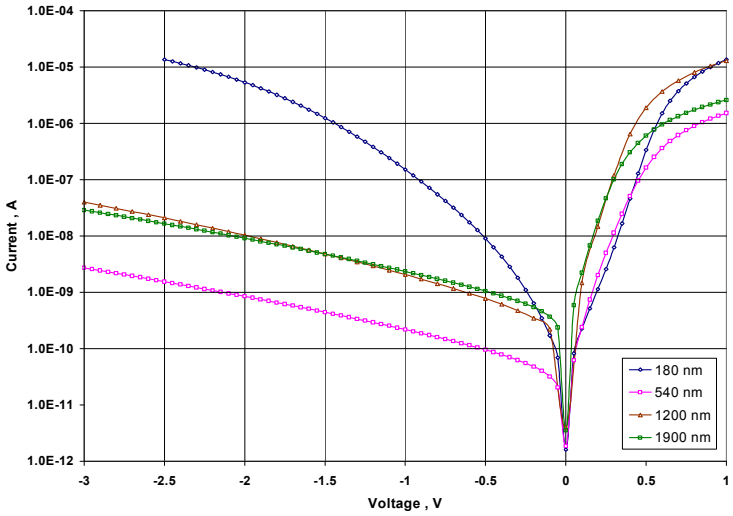


Figure 32. Dark current-voltage characteristics for p-i-n diodes made on oxidized silicon substrates. The thickness of i-layer is 180nm, 540 nm, 1200 nm and 1900 nm.

Figure 33 shows plots of rectifying ratio versus the thickness of the i- layer of the diodes fabricated on both glass-ceramic and oxidized silicon wafers. As can be seen from these figures, R has its maximum value when the thickness of i-layer is near 1000 nm. This value is probably correspondent to the optimal thickness in this structure. Higher thickness leads to increasing a series resistance of the i-layer that limits the forward current and gradually reduces the R value. Optical absorption measurements however, are required to measure and optimize effectiveness of these diodes as photovoltaic cells.

The fact that no difference was detected in behavior of the diodes fabricated on different substrates (oxidized silicon versus glass-ceramics) indicates that the barrier layer developed to coat glass-ceramics is meeting the objectives of the contract.

It should be noted that deposition of thick (above 1 micron) polysilicon films by low-pressure deposition (LPCVD) available at Cornell is not efficient (deposition at 620 C is relatively slow) and also does not fully utilize the high-temperature ability of glass-ceramic substrates. (Indirectly, the high temperature ability is used in the anneal used to improve the material, as well as in dopant activation). To deposit thick silicon films on barrier coated glass ceramics we started a collaboration with the group of Prof. Neudeck at Purdue University. We intended to use Purdue's high temperature APCVD reactor to deposit intrinsic silicon layer for our thin film solar cell prototypes. It turned out that a seed layer is required since silicon deposited by decomposing diclorosilane (DCS), the precursor used at Purdue, does not nucleate well on SiO_2[1]. This was a problem, as SiO_2 was on the surface of both our oxidized silicon control wafers as well as our barrier coated glass-ceramic substrates.

To fabricate thin film diodes (see **Figure 34**) we prepared substrates of oxidized silicon and barrier layer coated glass-ceramics with a 100 nm thick layer of heavily doped n+ polysilicon deposited at 620ºC by LPCVD. This n+ polysilicon film was patterned with photolithography to form the bottom contact of the final device. A thin (100 nm) layer of low temperature oxide (LTO) was then deposited by LPCVD and patterned to be later used as an etch stop during the etching of the i-layer. A thin (below 100 nm) seed layer of undoped polysilicon was also deposited at 620ºC by LPCVD (reasons for using undoped Si seed layer instead of nucleating directly on n+ Si bottom layer are considered in the following section). The wafers were sent to Purdue University where an approximately 2 micron thick layer of undoped silicon (i- layer) was deposited at 900ºC by APCVD. The samples were then shipped back to Cornell where we completed fabrication of the devices. To form a top contact a 100 nm thick layer of p+ doped polysilicon was deposited at 620ºC by LPCVD. The p+ and i- films were patterned by photolithography and dry-etched with RIE to form isolated devices. To activate the dopants, the wafers then were annealed in nitrogen at 900ºC for 4 hours. Aluminum contacts were thermally evaporated, patterned using lift-off technique and annealed in hydrogen at 400 C.

Measured dark I-V characteristics compared with the results measured on the similar devices (**Figure 35**), fabricated entirely at Cornell using the 620ºC LPCVD process to deposit i- layers, showed that the 900ºC devices had a lower series resistance, resulting in higher forward currents in the dark I-V and thus a higher rectifying ratio.

[1] This feature is exploited in the IC industry, where the diclorosilane reactor is used to deposit Si selectively on areas of the wafers where the underlying Si is exposed but not on areas covered with oxide.

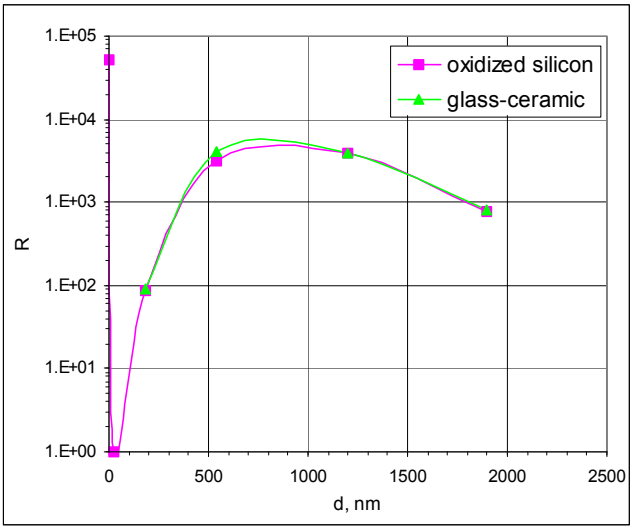


Figure 33. Plot of diodes rectifying ratios measured at 0.6 V bias versus thickness of the i-layer.

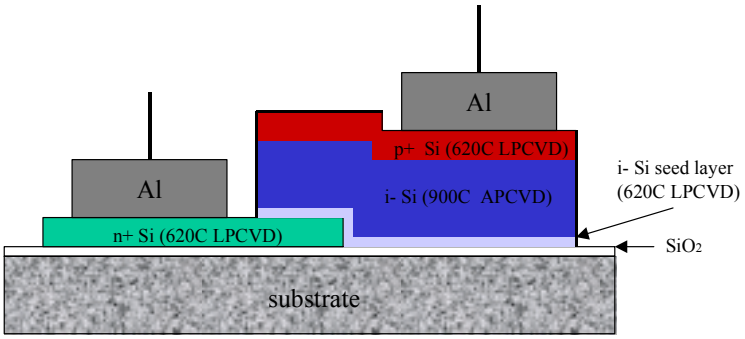


Figure 34. Schematics of the thin film solar cell prototypes fabricated at high temperature (900°C)

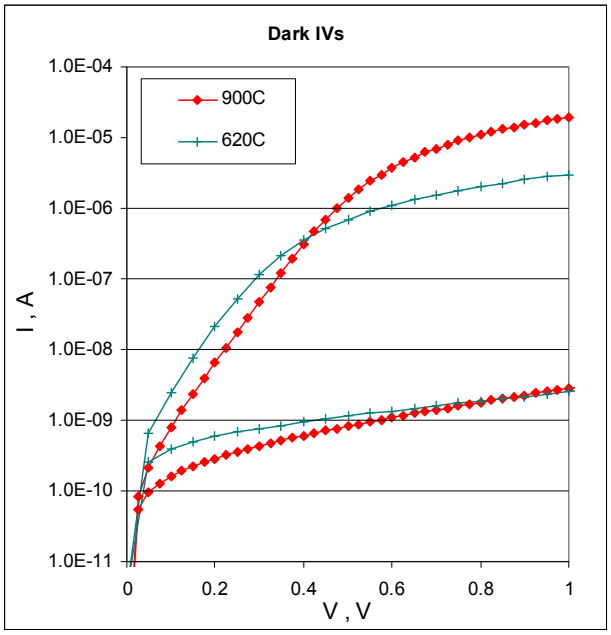


Figure 35. Dark I-V characteristics of the diodes fabricated at high (900ºC) and low (620ºC) temperatures.

5. Crystal Structure and texture of polycrystalline Si films.

- TEM analysis

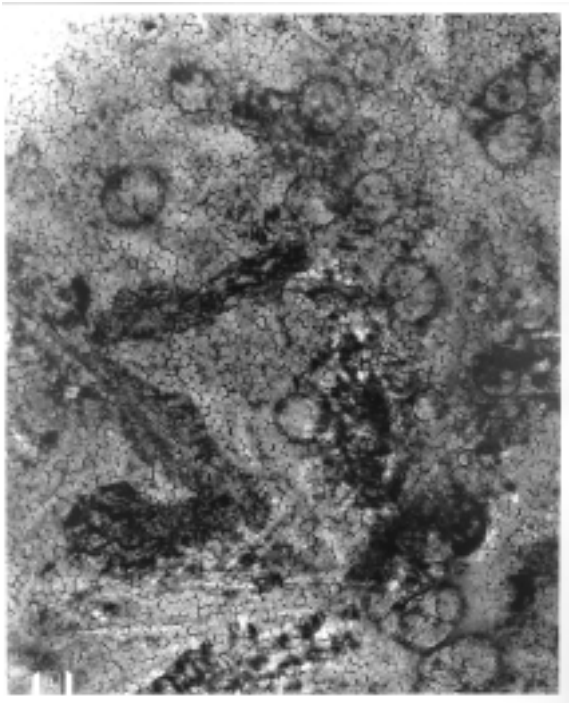
The structure of the polysilicon film deposited on barrier layer coated glass-ceramic substrates was investigated using Transmission Electron Microscopy (TEM) analysis. 1000 Å of amorphous silicon was deposited at 550 ºC and then recrystallized at 900 ºC. The film was patterned into 5x5 mm squares and then lifted from the surface to be imaged in TEM. In addition, cross-sectional specimens were prepared.

TEM study of cross-sectional samples confirmed that, after the annealing, the channel Si was completely recrystallized. The lateral size of poly-Si grains was similar for all three substrates and ranging from 100 to 500 nm.

TEM analysis of planar samples revealed the presence of a fine (30 nm) subgrain structure in all polysilicon films deposited on barrier coated substrates, regardless if the underlying substrate was fused silica or a glass-ceramic (**Figures 36a,b,c**). This fine structure was not present in the films deposited on uncoated fused silica. The formation of this fine structure was traced to the surface of the barrier layer where similar features were also found by AFM.

These results, again, indicate that the surface roughness and morphology of the barrier layer coated glass-ceramic substrates are important parameters determining both crystal and electronic structure of the deposited polysilicon films. They are consistent with the DOS results in that the presence of the subgrain structure is expected to increase the density of deep states in the film.

(a)



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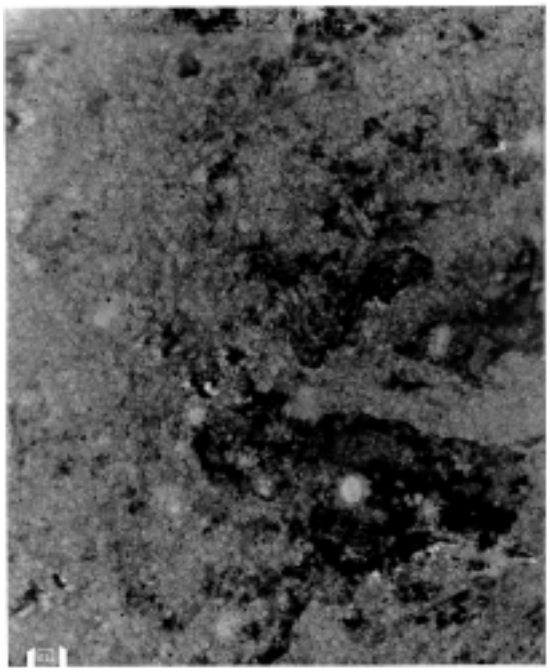


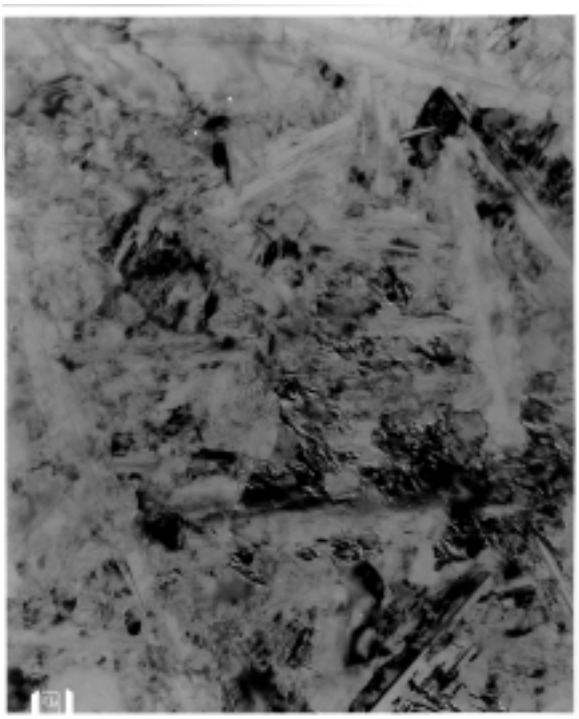
(c) 

Figure 36. TEM images of polysilicon films deposited on barrier layer coated glass-ceramics (a), barrier layer coated fused silica (b), and bare fused silica (c) substrates.

- X-ray analysis

The crystal structure and morphology of the thin polysilicon is known to have important influence of the performance of photovoltaic devices. Thin film, single layer polysilicon solar cells with {110} texture have better conversion efficiencies than cells with other crystallographic orientations[2].

To measure the crystallographic orientation polysilicon films deposited by APCVD at 900 C and to optimize the fabrication process we performed X-ray diffraction analysis. Two sets of samples were prepared for the analysis. In the first one, we deposited thin (100 nm) layers of n+ doped, and in the second one, undoped polysilicon by LPCVD as the seed layers for APCVD. The n+ layer is used as a bottom contact in our solar cells and we wanted to explore the feasibility to use it as a seed layer for the intrinsic silicon film [3]. 2 micron thick poly-Si layers were deposited on these seed layers at 900ºC using DCS in the APCVD reactor at Purdue University.

X-ray analysis revealed that APCVD films nucleating on the undoped seed layer had a very distinctive (110) orientation (**Figure 37**). The intensity of other reflections (including (111)) was at least two orders of magnitude lower than that of (110). The situation turned out to be different for the film deposited on the n+ seed layers. In this

[2] The likely reason for the low electrical activity is that tilt grain boundaries with {110} median planes, up to tilt angles of 108 degree do not contain broken bonds.

[3] N^+, phosphorous doped, poly-Si films have a considerably larger grain size than intrinsic films. Successful nucleation on n^+ films therefore will increase the grain size of the intrinsic layer.

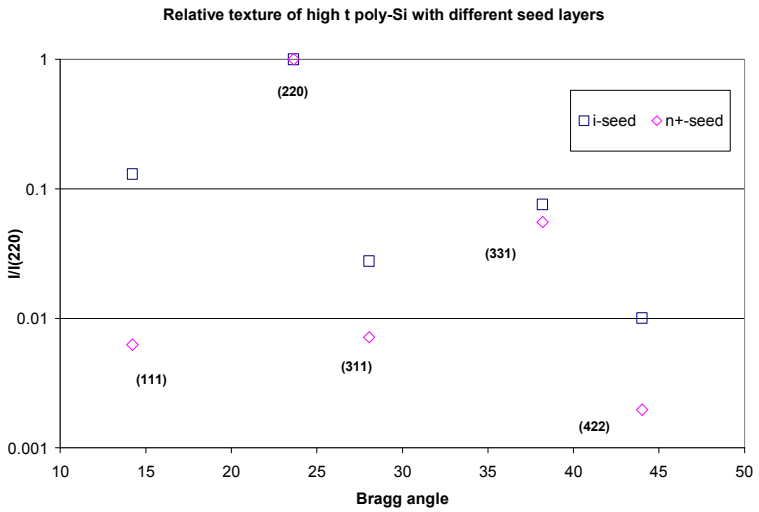


Figure 37. Relative intensities of X-ray reflections measured on polysilicon films deposited by APCVD using n+ doped (n+ seed) and undoped (i- seed) seed layers.

case, the degree of (110) texture was less. Noticeable intensity from (111) and (311) reflections suggests that the films deposited directly on n+ seed layer have less texture than those fabricated on the undoped seed layer. The difference can be traced to the influence of P, the addition of which changes the texture and increases grain size [11].

6. Monitoring of impurity migration through barrier layers by DLTS

In any future use of glass ceramic substrates for *large* grain polycrystalline solar cells, An important question is the ability of the barrier layer developed here to effectively suppress the out-diffusion of metallic impurities from the glass ceramic substrate. These impurities degrade the conversion efficiency of single crystal solar cells at concentrations as low as 1E14 cm^{-3}. [12-17]. The small grain polycrystalline solar cells tested in this program are relatively insensitive against this effect as the recombination at grain boundaries and defects inside grains is already high. The impurity concentration has to reach values of ~ 1E16 cm^{-3} to compete with this background. Commercially proposed small grain cells, therefore, are a) relatively impurity insensitive and b) designed conceptually similar to amorphous silicon cells collecting carriers from depleted regions. Large grain polycrystalline cells, however, are designed to collect from quasi-neutral regions and hence are as sensitive as single crystal cells [see 18]. As new methods are being developed to generate large grain polycrystalline films demands on the barrier layers will increase.

DLTS is a very sensitive technique that permits to measure traps in single crystal silicon down to concentrations 3 to 5 orders of magnitude below the level of the substrate doping. However, in our polycrystalline silicon films, which contain large number of traps originating from structural defects (grain boundaries, intra-grain defects), the sensitivity of DLTS to detect externally added impurities is significantly lower.

Therefore, rather than working with deposited poly-Si thin films, we used single crystal silicon wafers having a *tight mechanical contact* with the glass-ceramic substrates. The couple was annealed and the impurity level was then measured by DLTS, using Schottky diodes made on the silicon wafers. We have not seen this technique discussed in the literature for testing diffusion barriers and therefore provide some details below.

Being an electrical technique, DLTS provides data on the level (or levels) in the bandgap and their cross-sections, values which are known form many elements. However, in many cases, this is not sufficient to identify the element. A less known feature of DLTS is that it can provide data on concentration profiles as well, as it probes deeper regions at larger reversed bias. We have used this technique to measure profiles in the silicon wafers, and extracted diffusion coefficient of the impurity migrating into the silicon. Details can be found in the Ph.D. thesis of Krasulya [19]. Diffusion coefficients in Si vary widely and knowledge of a third parameter in many cases permits to identify the chemical nature of the unknown impurity.

We first used the technique to test the tube used to anneal glass and glass-ceramic substrates. These tests showed that the tube contained a very low background of Mg. Although this concentration was well *below* the value where it would impact the conversion efficiency of even *single* crystal solar cells given the data of Davies et al., we decided to clean the tube by flowing TCA, a chlorine compound, through it for 8 hours, at 1000 ^{o}C.

To evaluate the effectiveness of this cleaning step we carried out a DLTS analysis of CZ wafers[4]. annealed in the tube for 4 hours at 900°C The DLTS spectra was featureless throughout the entire temperature range probed, 78K to 350K. The absence of peaks indicates that the processed wafers were free of contaminants to better than $10^{12}cm^{-3}$. Having established a clean baseline, we then used DLTS to test our barrier layers.

To provide a reference for the effectiveness of the barrier, we first studied the out-diffusion from non-coated (i.e. bare) substrates by annealing at 900C for 10 minutes CZ wafers in tight mechanical contact with *bare* glass-ceramic substrates. Not surprisingly, the DLTS spectra of these wafers (**Figure 38**) showed two major peaks at all rate window settings. The stronger peak was very wide. Its width (spanning >200K) indicates that it did not represent a single level within the band gap but rather a superposition of different levels. Although the traps responsible for the peak could not be identified, the height of the peak sets an upper limit on their total concentration, which was deduced to be $\sim 10^{13}cm^{-3}$. Since this concentration is typical for the solid solubility limit in silicon of many of the impurities contained in the glass ceramic, it is possible that the experimental value represents the solubility limit of the impurity(ies), rather than a kinetic limit..

The test was then repeated using *barrier covered* glass-ceramics, using CZ wafer/glass ceramic couples annealed at 900C for 10 minutes. In this case, the wide peak found on bare substrates disappeared (**Figure 39**). Since the CZ wafers went through exactly the same treatment except that some were annealed on bare, and others on LPCVD barrier layer coated glass-ceramic, the broad peak clearly is caused by impurities diffusing from bare glass-ceramic and not due by "intrinsic" changes in the silicon

[4] We also used high purity FZ wafers but found that waferslip in these mechanically weaker substrates introduced crystallographic defects the DLTS spectrum of which interfered with impurity tracking. Thus, CZ wafers were used, even though their residual doping concentration was higher, lowering the detection limit to about $1E12cm^{-3}$.

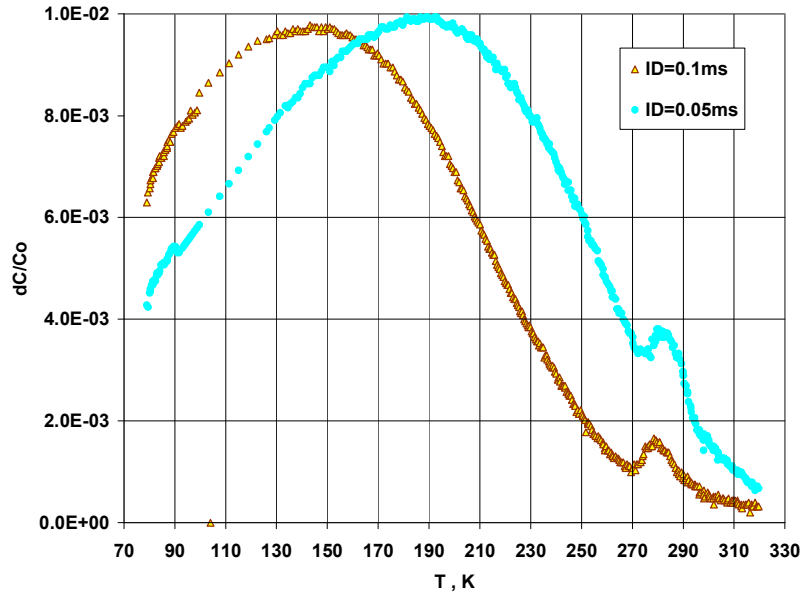


Figure 38. DLTS spectra for CZ silicon substrates annealed at 900°C for 10 minutes in direct contact with *bare* glass-ceramic substrate

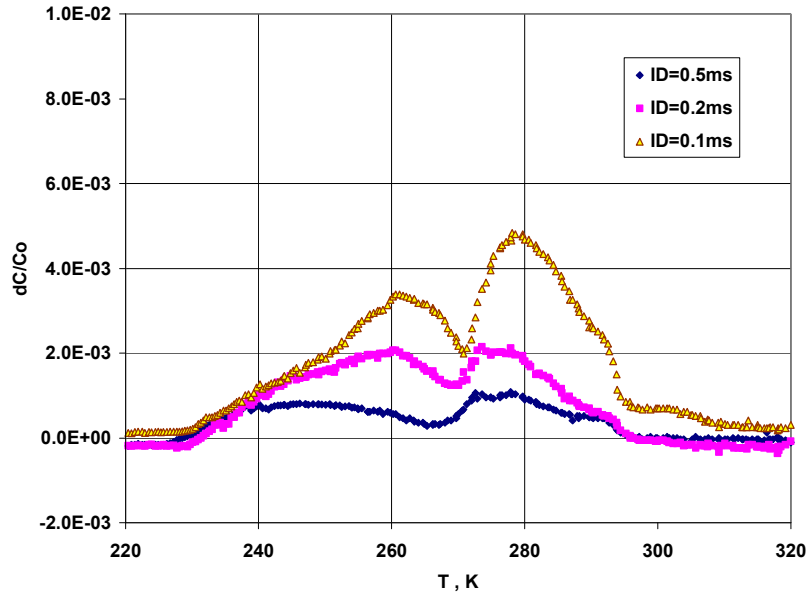


Figure 39. DLTS spectra for CZ silicon substrates annealed at 900°C for 10 minutes in direct contact with a LPCVD *barrier coated* glass ceramic substrate.

substrate [5]. The inverse rational suggests that the 270K-290K peak is "intrinsic", as it is similar in both figures. The DLTS spectra in Fig. 2 contain additional peaks in the range 230K-270K. The impurities responsible for these peaks were found to have strong temperature dependent capture cross-section, which hindered their identification. However, the total trap concentration represented is very low, ~3 $10^{12}cm^{-3}$. Considerably higher concentrations are needed to reduce solar cell efficiency, see the data of Davies et al [12-17].

We then increased the annealing time at 900 C by a factor of 240 to 4 hours. In wafers from such couples there are two DLTS peaks, located at the positions similar to those observed after a10 minute anneal (**Figure 40**). However, the peaks were higher than those after 10 minute anneal, which is consistent with the source of traps being diffused from the glass-ceramic substrate. However, even after this 2400 minute, 900C, anneal the concentration of out-diffused impurities remained well below that seen after a 10 minute anneal on *bare* substrate. Because of time restrictions (this work was done on a no cost extension), we did not extend these measurements to the double or triple barrier layers prepared in the program. But it is clear that this very sensitive technique will be useful should large grain, single junction solar cells on glass ceramic substrates become a reality.

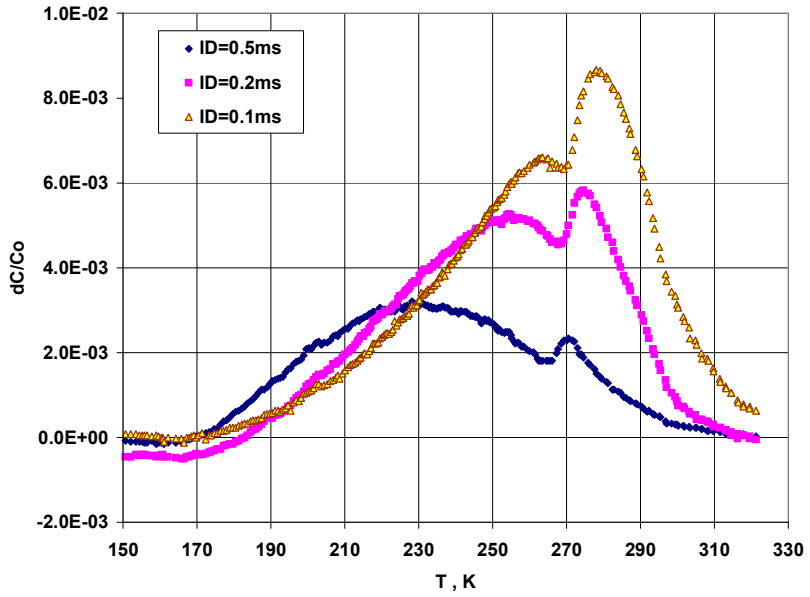


Figure 40. DLTS spectra for CZ silicon substrates annealed at 900°C for 4 hours in direct contact with a LPCVD *barrier coated* glass-ceramic.

[5] See footnote 4. At the low levels discussed here, it is relatively easy to generate states in the bandgap that are not related to impurities but from other sources such as wafer slip, changes in the point defect cluster population, oxygen precipitation etc.

7. Conclusions

This investigation showed that novel glass ceramic substrates, fabricated for this research with out charge by Corning Inc., are suitable to fabricate thin film silicon films at temperatures up to greater 900^{o}C; provided these substrates are covered with a simple two layer diffusion barrier, consisting of 100 nm of PECVD nitride and 100 nm PECVD oxide.

The performance of all devices, be it minority and majority carrier, fabricated on these barrier coated glass ceramic substrates was found to be identical to those of devices fabricated in the same run on oxidized silicon and fused silica control substrates. Second order variations in device performance were traced to differences in surface roughness, which tends to be higher on barrier coated substrates, and in the case of silica only, to its mismatch to the thermal expansion of silicon. Any future development of the already highly satisfactory barrier layer should be directed towards further reduction of its surface roughness.

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13. ABSTRACT *(Maximum 200 words)* This report describes how Cornell University researchers developed several low-cost and simple barrier layers and tested their effectiveness both analytically (by SIMS) and by evaluating the electrical characteristics of devices fabricated on barrier-coated substrates. Devices fabricated included both majority-carrier devices (thin-film transistors) and minority-carrier devices (p-i-n junction diodes simulating solar cells) using various deposition techniques including the chemical vapor deposition of polysilicon from silane at low pressures (at Cornell University) and from dichlorosilane at atmospheric pressure (cooperation with Neudeck at Perdue University). The structure of the films deposited was investigated by using TEM and X-ray analysis. The performance of the minority- and majority-carrier devices fabricated on barrier-coated glass ceramic substrates was found to be identical to devices fabricated on control substrates of oxidized silicon and fused silica.

14. SUBJECT TERMS: PV; glass-ceramic substrates; silicon solar cells; thermal expansion; barrier layers; thin-film transistors; p-i-n junction diodes; chemical vapor deposition; optical transparency; bias temperature stress (BTS); low-cost glass

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